

T.R.
GEBZE TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

**APPLICATION OF BIDIRECTIONAL AC-DC GRID
CONNECTED CONVERTER FOR HOME BATTERY SYSTEM, V2G
AND V2H OPERATION**

AHMET FARUK KANTEPE
A THESIS SUBMITTED FOR THE DEGREE OF
MASTER OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

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PROF. DR. ABDULKADİR BALIKÇI

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T.C.
GEBZE TEKNİK ÜNİVERSİTESİ
FEN BİLİMLERİ ENSTİTÜSÜ

V2G, V2H VE EV BATARYASI İÇİN
ŞEBEKEYE BAĞLI ÇİFT YÖNLÜ AC-DC
DÖNÜŞTÜRÜCÜ UYGULAMASI

AHMET FARUK KANTEPE
YÜKSEK LİSANS TEZİ
ELEKTRONİK MÜHENDİSLİĞİ ANABİLİM DALI

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GEBZE
2021

GEBZE TEKNİK ÜNİVERSİTESİ	YÜKSEK LİSANS JÜRİ ONAY FORMU
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SUMMARY

Market penetration of electric vehicles (EV) continues to grow. This growing brings some possible problems in the future for the existing electric grid system since electric vehicles carry huge batteries to be charged. In addition to this, renewable energy sources have fluctuating nature which is another growing industry. In order to cope with time varying supply and sink changes on the grid, distributed energy sources might ease stress on the grid.

In this thesis, a bidirectional AC-DC converter system has been studied. Unlike unidirectional AC-DC converters, bidirectional AC-DC converters can help reducing stress on the grid system by supplying current to the grid when needed. This thesis has two main chapters that divide AC-DC conversion and DC-DC conversion stages. For the AC-DC part, which is grid connected front end of the system, Totem Pole Bidirectional PFC converter is studied. Inductor and capacitor calculations have been conducted as well as control algorithm in Matlab-Simulink. For the DC-DC part of the system, Dual Active Bridge (DAB) converter has been studied. Power flow analysis and calculations for magnetics have been done including inductor and high frequency transformer. Control algorithm for DAB converter have been designed in Matlab-Simulink.

Key Words: Totem Pole, PFC, Dual Active Bridge, DAB, bidirectional, AC-DC converter.

ÖZET

Elektrikli araçların pazar payı gün geçtikçe artmaya devam ediyor. Elektrikli araçların taşıdıkları bataryalar büyük miktarda enerji depolayabildikleri için bu büyüme ileride elektrik şebekelerinde muhtemel bazı problemlere yol açabilir. Bununla birlikte, yenilenebilir enerji kaynaklarının da doğası gereği değişken miktarda enerji üretebilme kapasiteleri de göz önünde bulundurulduğunda, elektrik şebekesine bağlı dağıtık enerji kaynaklarının şebeke üzerindeki stresi azaltabileceği düşünülmektedir.

Bu tezde, çift yönlü AC-DC dönüştürücüler incelenmiştir. Tek yönlü AC-DC dönüştürücülerden farklı olarak çift yönlü dönüştürücüler, ihtiyaç halinde elektrik şebekesine akım aktarabildikleri için şebeke üzerindeki yükü hafifletebilirler. Bu tez ana başlıklar olarak AC-DC dönüştürücü ve DC-DC dönüştürücü olarak ikiye ayrılmıştır. Elektrik şebekesine bağlı uç için Totem Pole çift yönlü PFC dönüştürücü üzerinde çalışılmış olup, endüktans ve kapasitans hesaplamaları yapılmıştır. Bununla birlikte sistem Matlab-Simülink üzerinde gerçekleştirilmiştir. Sistemin DC-DC kısmı için Dual Active Bridge (DAB) dönüştürücü üzerinde çalışılmış, güç akışı denklemleri çıkarılmıştır. Bununla birlikte endüktans ve yüksek frekanslı trafo gibi manyetik parçaların hesaplamaları yapılmıştır. DAB dönüştürücü için kontrol algoritması Matlab-Simulink üzerinde gerçekleştirilmiştir.

Anahtar Kelimeler: Totem Pole, PFC, Dual Active Bridge, DAB, çift yönlü, AC/DC dönüştürücü.

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LIST of ABBREVIATIONS and ACRONYMS

<u>Abbreviations</u>	<u>Explanations</u>
<u>and Acronyms</u>	
CCM	: Continuous Conduction Mode
CRM	: Critical Conduction Mode
DAB	: Dual Active Bridge
DCM	: Discontinuous Conduction Mode
DP	: Dissipation Factor
DPF	: Displacement Power Factor
ESL	: Equivalent Series Inductance
ESR	: Equivalent Series Resistance
G2V	: Grid to Vehicle
Hz	: Hertz
OBC	: On Board Charger
pf	: Power Factor
PFC	: Power Factor Correction
SPST	: Single Pole Single Throw
V2G	: Vehicle to Grid
ZVS	Zero Voltage Switching

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1. INTRODUCTION

1.1. Scope and Motivation

Over the last decades, concerns about usage of petroleum and its refined oil variants as an energy source have been rising. Petroleum consumption causes significant CO₂ emission that causes global warming. In order to keep CO₂ emission under control, almost 200 countries have declared intention to lower greenhouse gas emission thus signed Paris Agreement at 2015 United Nations Climate Change Conference (COP21) [1]. Petroleum is the primary energy source for almost any vehicle for consumers. In this regard, lowering greenhouse gas emission of vehicles might help to reach this goal.

Electric light vehicle sales percentages quadrupled since 2015 [2], which is the date of the Paris Agreement. Also, electric vehicle sales have passed 50% mark in Norway [3] in 2020. Growing market share also requires a good charging strategy. Since electric vehicles have big batteries, the energy demand for charging may triple average monthly electric consumption [4]. Therefore, grid friendly charging systems for electric vehicles can improve EV transition from internal combustion (IC) vehicles by helping EV ownership experience.

There are three levels of chargers that are defined by International Electrotechnical Commission (IEC) in IEC 61851-1 standard [5]. Levels of chargers according to publication by IEC are

- Maximum 3,7kW, domestic usage.
- 3,7kW to 22kW, up to 3 phase, for private and public chargers.
- More than 22kW, AC or DC, public chargers.

There are four modes of charging defined by IEC. Briefly, it keeps the first two levels of chargers and divides the last level of the charger into two as AC and DC operating ones [6]. Therefore there are two modes of charging for >20kW charger as AC or DC.

Practically, only Mode 1 or Mode 2 charging can be implemented in OBC. Thus, improvements on OBC can have a big impact on sustainable large scale EV adoption

as well as grid health. The electric vehicle industry grows fast but the capacity and reliability of the current grid infrastructure is a big question. Since electric vehicles are considerably big loads for the grid, some precautions need to be made in order to keep it safe and uninterrupted. That being said, distributed power sources could ease balancing the grid. Bidirectional AC-DC chargers are grid friendly option for electric vehicles that can act as a distributed power source. They can both supply current to the grid or draw current from the grid to charge electric vehicles.

In this thesis, a complete design solution for a bidirectional AC-DC converter will be examined.

In this study, a bidirectional AC-DC converter will be implemented to develop a platform that is capable of bidirectional power flow between grid and any system which needs high voltage DC. From this point of view, home batteries, electric vehicles, and other types of energy storage systems are a good candidate for this. Moreover, step by step design stages of a bidirectional AC-DC converter will be realized and the basics of selected topologies will be explained.

1.2. Thesis Contributions

The study in this thesis will be focused on two stage AC-DC converter. Thus AC-DC and DC-DC converter design will be separated. After that, those converter designs will be combined to create a flexible bidirectional AC-DC converter. Topology reviews will take place and convenient ones will be put together.

The main goal of this thesis is to develop a platform that is capable of interfacing distributed energy sources and connecting them to the grid infrastructure. In this thesis, AC-DC converters will be examined in terms of on board chargers and home battery charges as they function very similarly. Therefore, OBC term will be used as a common term of both.

2. LITERATURE REVIEW of AC-DC CONVERTERS

2.1. Power Factor Correction (PFC) AC-DC Converters

OBC AC-DC converters can be divided into two distinct sections, an AC-DC converter, and a DC-DC converter [7]. Generally, the AC-DC converter is responsible to draw current from the grid while consuming less reactive power possible. This is known as power factor correction (PFC) that shapes input current drawn from the grid in phase with the grid voltage. Without a PFC converter, it not possible to satisfy electrical regulations enforced by the governments. Thus, PFC converters are de facto standard for OBC therefore, non-PFC AC-DC converters are out of our scope. Following DC-DC converters are implemented for isolation and charging profile purposes. It enables flexible voltage output as well as power flow. Isolation is a key safety measure because high voltage and high current are being implemented.

Most used AC-DC PFC converters can be tabulated as below

Table 2.1: Key components used in various PFC converters.

	Conventional boost PFC	Bridgeless boost PFC	Totem pole PFC	Full bridge (Totem Pole) boost PFC
Inductor	1	1	1	1
Slow diode	4	0	2	0
Fast (boost) diode	1	2	0	0
Switch	1	2	2	4

In addition to those tabulated, there are interleaved variants that implement numbers of copies of the associated topology and runs them in phase shifted manner.

Conventional boost PFC uses four diodes for rectification and one switch for boost function. Boost function has control over input current so can make it in phase with the input voltage, lowering harmonics thus reactive power demanded from the

grid. Figure 2.1 (a) shows a conventional boost PFC converter [36] and (b) an interleaved variant [26].

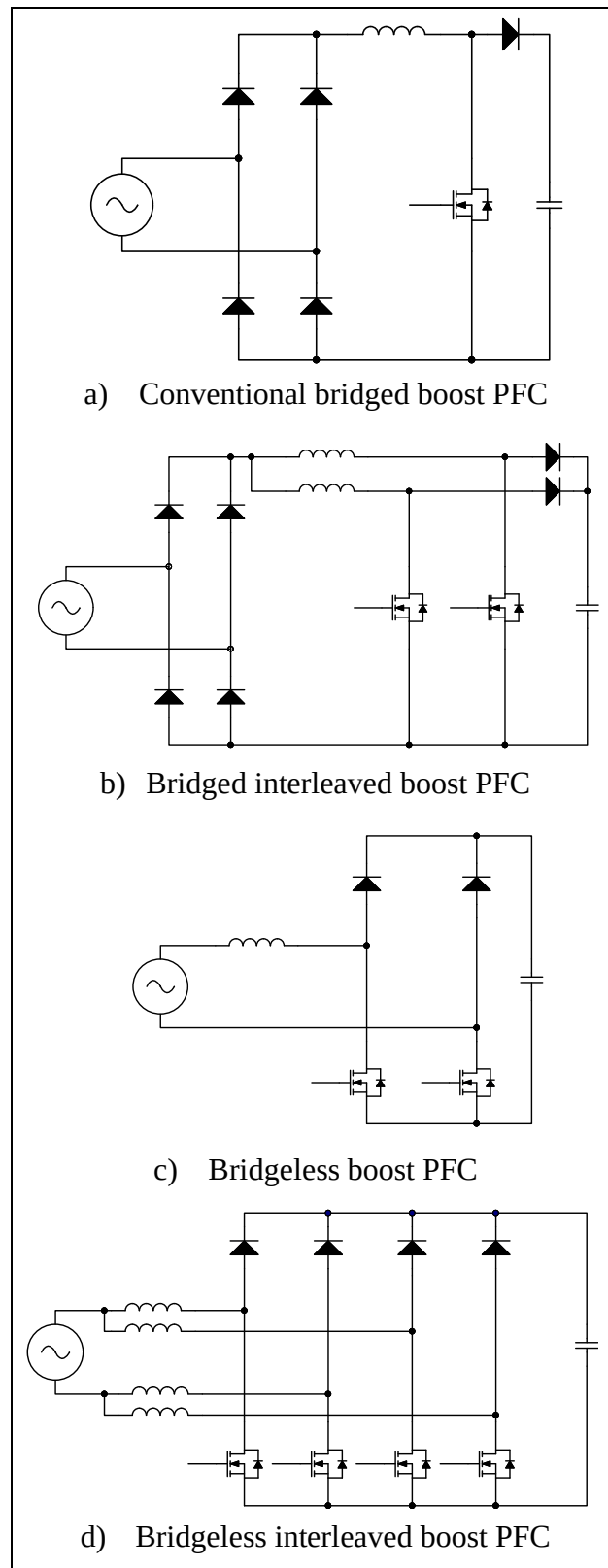


Figure 2.1: Various boost PFC converters.

In a conventional boost PFC converter, bridge diodes have forward voltage drops that cannot be avoided, resulting in a predictable and linear loss. In addition to this, the boost diode also has a forward voltage drop which contributes to power loss. Furthermore, reverse recovery loss is also a significant factor of loss parameter. However, only one dedicated switch is being implemented in this topology, makes it the easiest method for PFC.

To further improve efficiency, the bridgeless boost can come in handy. Since it eliminates rectifying slow diodes and adds another switching device that effectively divides one grid cycle into two. One switch is responsible to boost the positive cycle of the grid voltage and the other switch is responsible to boost the negative cycle of the grid voltage. Therefore, the average current stress on switches is halved. Figure 2.1 (c) shows a typical bridgeless boost PFC converter. Despite the lowered average current, the peak current flowing through the boost inductor and booster switch is the same as the bridged variant. This enables higher power output at a cost of two equally strong booster switch in terms of peak current capability.

Bridgeless totem pole PFC can improve bridgeless boost PFC converter by rearranging switch and transistor positions, effectively making it synchronous boost converter. This eliminates two fast diodes and its reverse recovery drawback resulting in higher efficiency possible. However, line rectification is ensured by slow diodes, so this topology is not capable of bidirectional power flow. Figure 2.2 shows two different totem pole topologies.

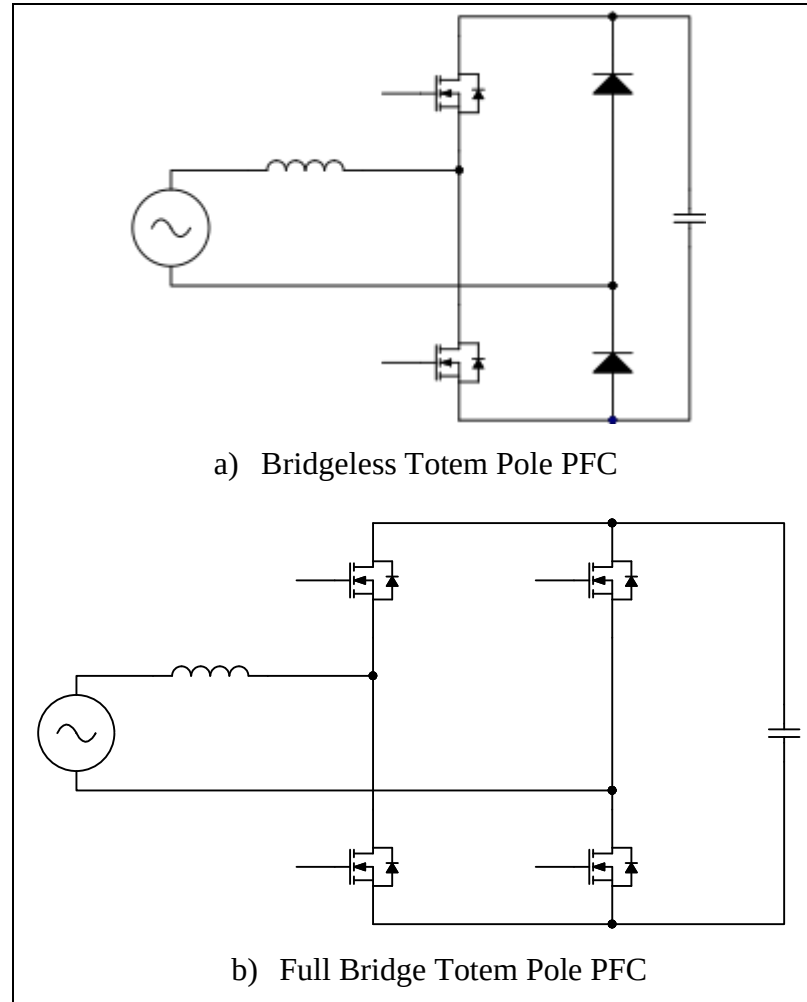


Figure 2.2: Totem Pole PFC converters: a) classical Totem Pole PFC with diodes for line rectification b) improved Totem Pole PFC, diodes replaced with switches for bidirectional flow.

In order to support bidirectional power flow, diodes should be eliminated, since they strict current conduction in one way or additional switches should be implemented. A PFC converter in [8] has been purposed with the line rectification diodes replaced with transistors. However, it requires additional 4 switches along with interleaved bridgeless totem pole configuration in [27]. This makes it slightly harder to control. Additional cost of gate drive circuitry is another drawback.

Bridgeless bidirectional totem pole PFC converter is another popular choice of PFC method since it employs fewer switches compared to study in [8] and zero diodes. Furthermore, big IC manufacturers like Texas Instruments, ST microelectronics, NXP, and Infineon are the companies promoting this topology. For this purpose, diodeless totem pole PFC converter is the obvious choice of our use case since diodes are not implemented and fully controllable four switches formed in full bridge configuration

can inherently enable bidirectional capability. This topology is well studied among the other PFC topologies as a part of OBC.

Bridgeless bidirectional totem pole PFC topology is further improved in many studies with using Gallium Nitride (GAN) fets. It has superior performance among the other switches. Furthermore, it does not have an inherent PN junction, that is called body diode for other fet based switch structures, which eliminates reverse recovery issue completely. Despite this superior performance shown by GAN switches, the technology is rather new and should prove its reliability before using in an automotive application. As of this thesis is being completed in Q1 2021, few manufacturers were able to supply AEC-Q101-qualified GAN fets. Texas Instruments is the first manufacturer that can produce automotive grade GAN switches with an integrated driver, with a voltage rating of 650V and 600V, just announced in Q4 2020.

Another big leap forward is Silicon Carbide (SiC) Mosfet which enables higher efficiency. There are manufacturers in the market supporting automotive grade applications with breakdown voltage of 1700V and higher. Furthermore, considering the immaturity of GAN, and the superiority of SiC FET over silicon fets [18], we selected to use SiC FET switches.

2.2. Isolated DC-DC Converters

DC-DC converters are one of the well-studied power electronics topics. There are quite different kinds and techniques studied, including novel designs. Despite very diverse kinds and topologies are being studied [20], there are few topologies within the context of OBC that have been widely adopted by the market giants. If isolation was not a concern, classical topologies such as buck-boost [21], cuk [22], sepic [23], etc. could be implemented easily with minor tweaks and adjustments since those topologies have become vastly mature and there are plenty of analog and digital controllers designed by industry leaders. Moreover, those implementations can also eliminate using the standalone PFC part of the overall converter.

Since isolation has not been implemented in the PFC section, the isolation requirement should be satisfied within the DC-DC converter stage. Therefore, non-isolated DC-DC converters are out of our scope. Additionally, there are embedded converters that employ AC motor windings and traction inverter switches [9], [10].

Those kinds of topologies deserve a holistic approach to the power electronics infrastructure of the vehicle, therefore, will be kept out of scope.

LLC converters can be very promising since they can run at very high frequency with easily achieved soft switching operation, but they have a lack of flexibility in terms of reverse operation as it has a maximum voltage gain of 1[25]. They have very limited voltage gain when operated in V2G mode, limiting usefulness, as the 220-240VAC grid is adopted in most of the regions. Considering 325V peak voltage of 230VAC grid, low voltage battery might be a bottleneck for V2G operation.

Despite various topologies and sophisticated control schemes, there are few numbers of isolated DC-DC converter topologies adopted by automotive industries. One of them is Dual Active Bridge and the other one is CLLC Resonant Converter [11].

CLLC [19] and DAB [14, chapter 2: 2.1] converters may seem similar despite series capacitors, however, their control algorithm is quite different. CLLC converter is a resonant converter hence, the main control parameter is switching frequency. Figure 2.3 shows the basic structure of DAB and CLLC topology.

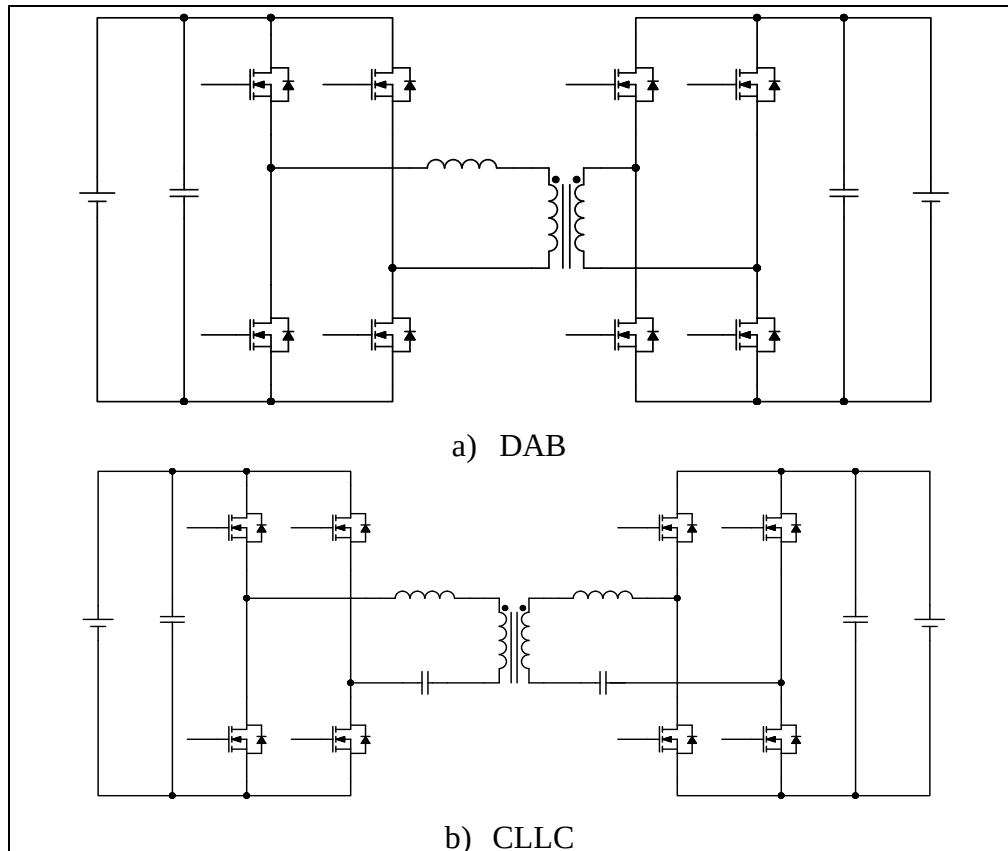


Figure 2.3: High power isolated DC-DC converter: a)DAB, b) CLLC.

CLLC converters have various advantages including efficiency and volume showed in studies [12], [13]. They tend to run at higher frequencies because of the wider ZVS range. The higher frequency capability of the CLLC allows designing much smaller magnetics and capacitors. However, the control strategy and output voltage adjustment are rather difficult compared DAB converter.

Table 2.2: Comparison of DAB and CLLC.

	Density	Current Stress	Switching Loss	ZVS	Ohmic Loss	Frequency	Complexity
CLLC	Higher	High	Low	High	High	Higher	High
DAB	High	Moderate	High	Moderate	Moderate	High	Moderate

DAB converters have quasi-square inductor current, and CLLC converters have quasi-sinusoidal inductor current with higher peak currents compared to DAB. This yields higher conduction losses. Despite the conduction loss drawback of CLLC, the converter can perform ZVS quite easily which gives better switching loss characteristics against DAB. However, DAB converters turn off at maximum inductor current which causes high switching losses.

DAB topology is the most used technique for high power and high frequency DC-DC converter. Additionally, power flow control and output voltage adjustments are quite easy on the DAB converter. For this flexibility, the DAB converter shall be our study topic. Discussion about CLLC and DAB will also be elaborated in relevant section 3.1.

3. DC-DC CONVERTER

3.1. Overview

DC-DC converters can be divided into two sections, isolated and non-isolated. Isolation is a crucial safety measure for high power converters. It also helps interfacing with two different power domains, eliminates return potential/zero voltage differences.

The overall system will need strong electrical isolation. As can be seen in section 4.2, the selected topology does not feature any isolation. Thus, isolation must be done in the DC-DC section of the system to achieve isolation between input and output. Therefore, only isolated DC-DC converters will be our subject.

Our subject is also getting bidirectional operation in order to achieve V2G and G2V power flow. Considering high output power and buck-boost requirements, CLLC resonant converter and DAB converter are the most popular topologies. Both topologies may be designed half bridge or full bridge configuration.

High power conversion brings some problems to overcome. Switching losses, conduction losses, magnetic losses, and thermal management are some of them. Since hard switching causes excessive power loss on switching devices because of finite switching slew rate along with finite ohmic resistance, it is very important to eliminate hard switching as much as possible. Additionally, due to excessive power loss on switching devices, serious precautions must be taken to cool down the devices. This also renders mechanical design cumbersome. Hard switching also brings EMI problems to solve. Hence, the highest soft switching needs to be achieved.

Bidirectional CLLC has many benefits including soft switching, which is a significant factor of high voltage, high power converters. However, the design process and control strategy is a lot harder. Bidirectional DAB topology is rather easy to design and control at a price of low load inefficiencies due to unavoidable drift to hard switching zone. Since the bidirectional AC-DC converter studied in this thesis would be used in electric vehicles, charging stations or home battery systems, the dynamic range of power demand is expected to be rather narrow. In fact, demanded power range is expected to be between roughly half to full power of the designed system. This design consideration eliminates low load inefficiencies of DAB at low load. As a result, Dual Active Bridge topology is studied in this thesis.

3.2. Selected Converter Method: Dual Active Bridge

This method is widely studied by many researchers. It contains a high frequency transformer along with an inductor in series with one of its windings. Full bridge circuitry made of four switches is present at both ends of the transformer. This makes the topology highly symmetrical, thus makes the design easier and enables it to perform bidirectional capability[14, chapter 2: 2.1]

High voltage, high power conversion methods always welcome higher switching frequencies. High frequency operations simply shrink down reactive energy storage elements, inductors, and capacitors, in volume. Thus, enables us to design highly compact devices. Transformers also benefit from high frequency.

Real world circuit components suffer from parasitic components. For example, capacitors have inductors and inductors have capacitors, as a parasitic component. Furthermore, switching devices also have parasitic components among its terminals. However, as switching frequency increases, magnetic components like inductors and transformers becomes harder to design due to inevitable stray components in them. For instance, parasitic capacitance in an inductor limits its maximum operable frequency. Both manufacturers of magnetic components and power electronic designers need to cope with the undesired effects of high frequency operation. In this thesis, these challenges are not our scope.

3.2.1. Topology

As stated in the previous section, the DAB converter consists of four switches on both sides, an inductor, and an insulating transformer. Considering power efficiency, the switches must perform soft switching to lower the total inefficiency of the whole system. Zero Voltage Switching (ZVS) works in such a way that, inductive and capacitive loads of the system nullifies each other so that the voltages on the switching devices are close to zero at the switching action. Thus, it enables soft switching.

Since high voltage and high frequency operation is always welcomed, wide bandgap (WBG) transistors such as Gallium Nitride (GaN) and Silicon Carbide (SiC) transistors are the perfect fit for our use case. Those devices exhibit better switching

capabilities thanks to lower input capacitances. Additionally, SiC and GaN devices can operate well on high temperatures while maintaining a modest rise in on resistance [37].

Basic schematic of DAB topology is shown in Figure 3.1 with MOSFETs as a switch.

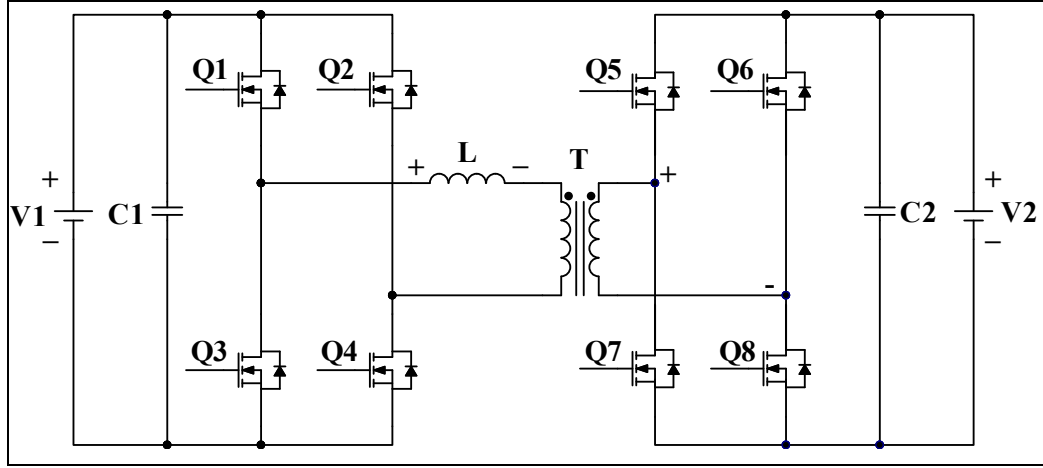


Figure 3.1: Schematics of Dual Active Bridge (DAB).

In order to get power flow, inductor and transformer should be fed with AC voltage. Switches on both sides are arranged in full bridge manner, thus capable of supplying the required AC voltage.

3.2.2. Phase Shift Modulation

DAB converters can be modulated with various parameters such as frequency, phase shift and duty cycle. However, phase shift modulation [29] is the most popular one among the others because the implementation is rather easy [28] thanks to simple control loop architecture.

There are four switches on each side of the high frequency transformer, functioning as a full bridge with a duty cycle of $D = 1/2$. As the name indicates, there is a phase shift ϕ between two bridges, allowing power flow from one to the other.

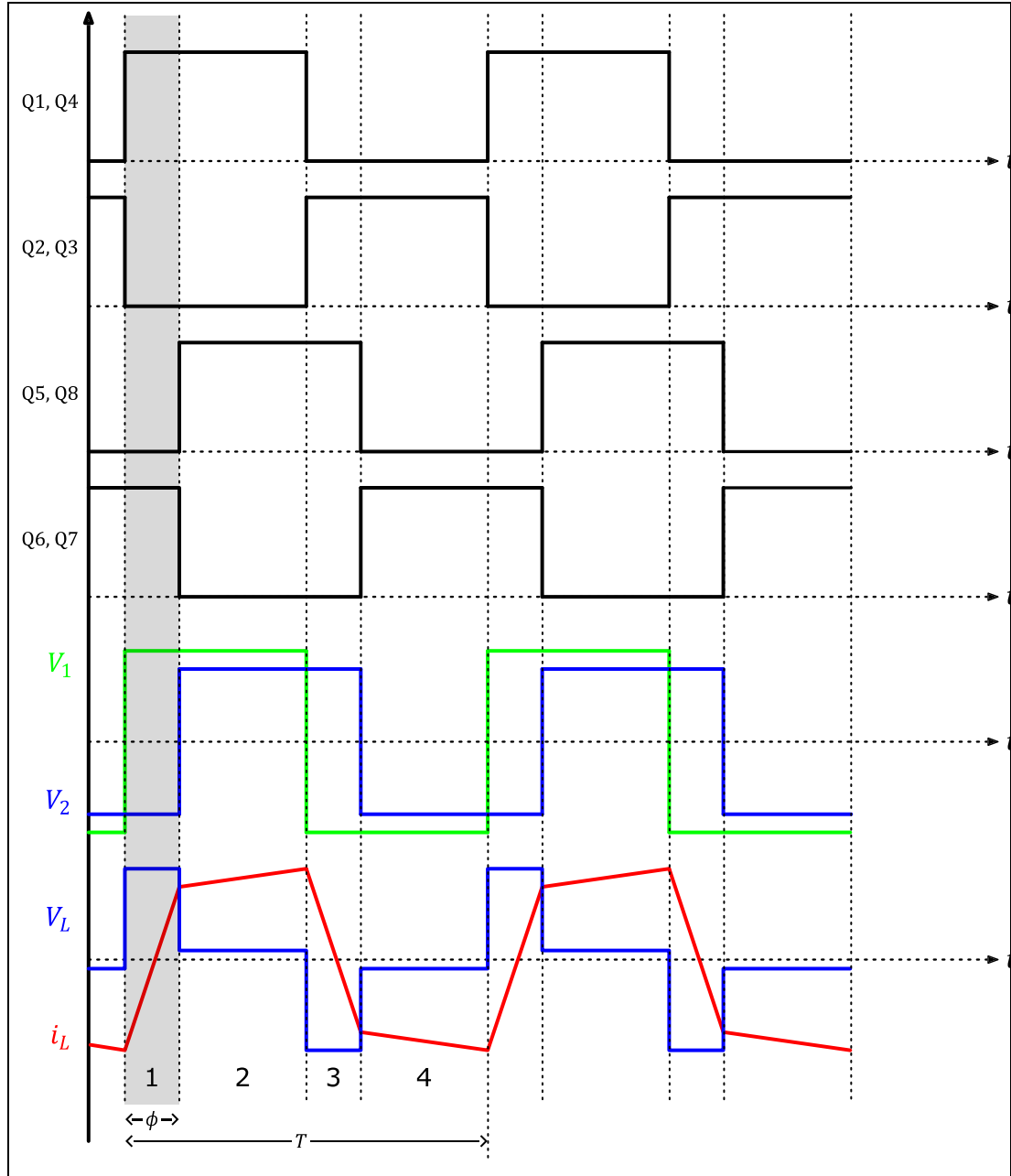


Figure 3.2: Key waveforms for Dual Active Bridge.

Switching states of two full bridges with phase shift and the inductor current is shown in Figure 3.2. In state 1, Q1 and Q4 turn on and applies a positive voltage to the inductor thus the transformer. During state 1, the secondary side applies a negative voltage to the transformer. Hence much bigger voltage difference appears on the inductor which makes the inductor current rise quickly. In state 2, the secondary side changes the polarity of the applied voltage to the transformer, thus effective voltage difference on the inductor becomes lower. Since the inductor current is created

according to voltage difference on it, the inductor current may be in a rising or falling fashion according to boost or buck operation. When boost operation is performed, the inductor current starts to fall. Similarly, when buck operation is performed, the inductor current continues to rise since the positive voltage is present anyway. In state 3, the primary bridge changes applied voltage to the inductor. Therefore, current starts falling or falls harder. Finally, in state 4, the secondary bridge starts to apply negative voltage thus lowers the effective voltage on the inductor. As mentioned earlier, the slope of the inductor current in state 4 might be positive or negative according to buck or boost operation. When Figure 3.3 [31], [32] is examined, it is very clear that state 3 and 4 is symmetrical to state 1 and 4 respectively. In fact, there are only two conditions that are happening whilst phase shift is present. The first one is that both bridges apply the same polarity to the transformer, and the second one is that the bridges apply opposite polarity to the transformer. Using this, calculation of power flow can be observed as the voltage and the current waveforms are available. Considering the ideal, lossless operation of the DAB circuit, switches can be replaced by AC voltage sources and high frequency transformer can be subtracted by reflecting its secondary side to the primary side.

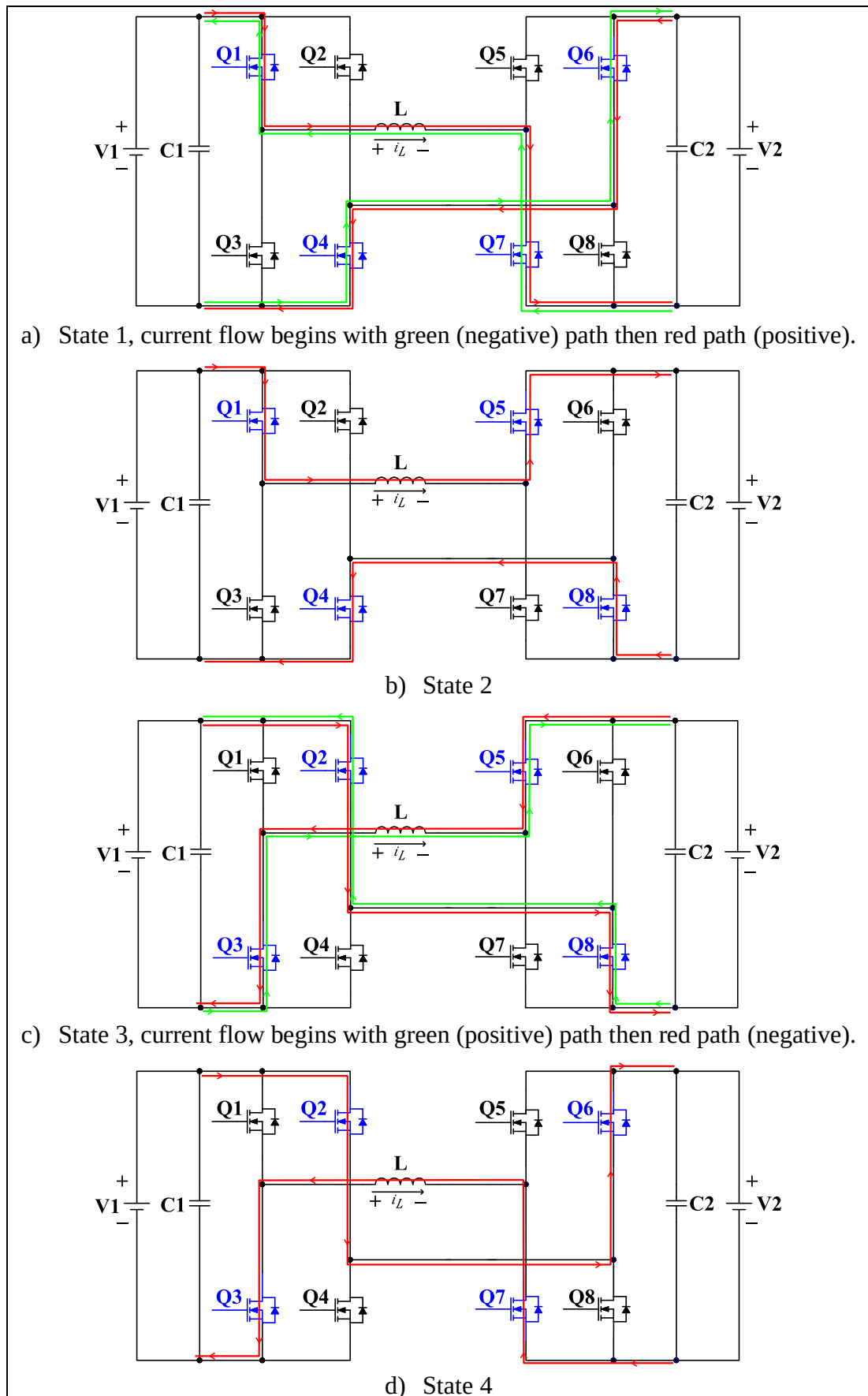


Figure 3.3: Current flow of DAB, divided into 4 states.

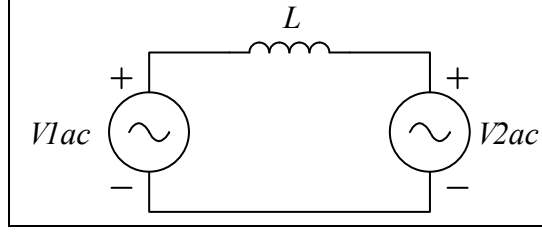


Figure 3.4: Simplified schematics of Dual Active Bridge.

Using circuit in Figure 3.4, the power transfer is:

$$P_{1-2} = \frac{1}{T} \int_0^T P_{1-2}(t) dt \quad (3.1)$$

Since we know current and voltage levels, Eq. 3.1 can be transformed to

$$P_{1-2} = \frac{1}{T} \int_0^T V_1(t) i_1(t) dt \quad (3.2)$$

It is easily distinguishable that the voltage and current levels are symmetric at every half cycle $T/2$, so that calculating power for half cycle and multiplying it by two would yield total power transfer.

$$P_{1-2} = \frac{2}{T} \int_0^{T/2} V_1(t) i_1(t) dt = \frac{2V_1}{T} \int_0^{T/2} i_1(t) dt \quad (3.3)$$

Easily seen that all parameters of Eq. 3.4 is constant except for the current. Nevertheless, the current function can be determined as a piecewise function with the help of a simplified circuit in Figure 3.4 and waveforms in Figure 3.2.

$$0 < t < T_\phi \quad : \quad i_L(t) = i_{L,0} + (V_1 + nV_2)t/L \quad (3.4)$$

$$T_\phi < t < T/2 \quad : \quad i_L(t) = i_{L,T_\phi} + (V_1 - nV_2)(t - t_1)L \quad (3.5)$$

Finally, recalling Eq. 3.3 and rearranging it with derived expressions in Eq. 3.4 and Eq. 3.5, the power transfer function becomes

$$P = \frac{nV_1V_2\phi(\pi - |\phi|)}{2\pi^2fL} \quad (3.6)$$

Where

- n : number of *primary turns/secondary turns*
- V_1 : Voltage on the primary side of the transformer
- V_2 : Voltage on the secondary side of the transformer
- ϕ : Phase shift in radians
- f : Switching frequency in Hz
- L : Total series inductance (leakage + any additional) in Henry

It is obvious that phase shift ϕ has a direct effect on power transfer. Therefore, phase shift to power transfer curve can easily be obtained by fixing all other parameters. Additionally, it is very clear that phase shift is meaningful between $-\pi/2 < \phi < \pi/2$ since it covers full dynamic range of power transfer capability of a phase shifted DAB.

3.2.3. Zero Voltage Switching (ZVS)

High power converters always pursue high power efficiency. One of the major loss parameter is switching losses. Hard switching can contribute substantial loss if not handled properly. For this reason, hard switching should be avoided as much as possible.

Hard switching happens when an electric potential is present on each leg of the switching device, for example, drain and source leg of a MOSFET, in our case. Since practical MOSFETs have non-zero rise and fall times, voltage and current flow curves can be present on MOSFET at the same time, resulting in intersections that represent hard switching losses. This causes ohmic losses on switching devices and generates heat that should be dissipated.

As the name implies, zero voltage switching tells that no voltage is present on switching devices. Thus no energy is dissipated during switching. In DAB topology, zero voltage switching is achieved in a resonant circuit manner. Series inductor in the DAB circuit and parallel capacitances on each switching device forms a resonant circuit. These capacitances may be parasitic capacitances as well as additional snubber capacitances. In switching events, series leakage inductor is responsible to discharge those capacitances thus, zero voltage on switches is ensured. In order to achieve ZVS, series inductance must store enough energy to discharge resonant capacitances.

In normal conditions, when the voltage transfer ratio is equal to 1, zero voltage switching is observed. The voltage transfer ratio represents normal output to input voltage ratio, with the transformer turns ratio is considered.

$$M = \frac{V_2}{nV_1} \quad (3.8)$$

However, when the converter operates at a low load, ZVS may not be achieved. For DAB converters, ZVS is achieved when [28]

$$d \geq \frac{M-1}{2M} + 2\sqrt{LC_i} \quad (3.9)$$

$$d \geq \frac{1 - M}{2} + \frac{2Mn\sqrt{LC_o}}{T} \quad (3.10)$$

Where C_i is leading(input) leg and C_o is lagging(output) leg of the bridge.

C_i and C_o can be estimated with C_{oss} value given in MOSFET datasheets. However, C_{oss} is fairly nonlinear thus if precise ZVS behavior is desired then in-depth simulation should be conducted.

3.3. System Design of Dual Active Bridge

Our use case targets home batteries, EV batteries, and any distributed energy systems such as solar farms with energy storage capability. Therefore, 400V on the secondary DC side is chosen. The primary side that will interact with the AC-DC converter is single phase. Considering 230VRMS mains voltage with a peak amplitude of 325V it can be boosted rather easily to a voltage level of 400VDC. Hence, 400V on the primary side also seems logical. Therefore, primary to secondary transformer ratio $n = 1$ inherently.

The phase shift is such an important parameter since the modulation method is founded on it therefore it needs to has stable and predictable effect on output power.

When inspecting Eq 3.6, phase shift to power transfer function is somewhat linear between $-\pi/6 < \phi < \pi/6$. Outside of this range, phase shift to power transfer ratio has diminishing returns. Additionally, the linearity of the power transfer function would be disrupted. Therefore, the maximum phase shift at maximum design power is decided to be $|\phi| < \pi/6$. All key parameters are tabulated as follows.

Table 3.1: Design parameters of DAB.

Parameter	Value
Design Power	1KW
Input Voltage	400V
Output Voltage	400V
Output Current	2,5Arms
Switching Frequency	100kHz
Phase Shift(max)	$\pi/6$

Since the inductor is the only element that enables power transfer, it is logical to design it in the first place. Therefore, we can recall power transfer Eq 3.6, rearrange it to find the required inductance, and plug the values in Table 3.1 we calculate the inductance value as;

$$L = \frac{nV_1V_2\phi(\pi - |\phi|)}{2\pi^2fP} = \frac{1 \cdot 400 \cdot 400 \cdot \frac{\pi}{6} \cdot \left(\pi - \frac{\pi}{6}\right)}{2\pi^2 \cdot 100 \cdot 10^3 \cdot 10^3} = 111,111\mu H \quad (3.11)$$

3.3.1. Inductor Design

A good magnetic design is always iterative and requires good guesstimate. There are too many variables and tradeoffs, for example, maximum magnetic field, temperature, frequency, DC-bias, parasitics, and so on. Therefore, the design process is multi-dimensional and might be overwhelming. Thus following calculations are conducted under likely non-ideal assumptions and arbitrary choices, although it is good to start with theoretical equations.

First, the designed inductor must store the required energy. Therefore, it is a good start to calculate energy storage requirement. Stored energy in an inductor can be calculated as

$$E = \frac{1}{2}I^2L \quad (3.12)$$

Where I is current flow and L is inductance.

Since inductors store energy in a medium, in our case it is ferrite core, we need to know how much ferrite material is needed. The volume of magnetic material with known effective permeability can be expressed as

$$V_{e,min} = \frac{\mu_e\mu_0E}{B_{sat}^2} \quad (3.13)$$

Where μ_e is effective permeability denoted by core manufacturer or calculated from μ_i initial permeability according to airgap introduced in a magnetic circuit, μ_0 is

permeability of free space, E is stored energy in inductance and B_{sat} is saturation magnetic field denoted by core manufacturer.

Effective permeability μ_e can be obtained from manufacturer's datasheets. However, for most ferrite materials, it is too big for a power inductor which leads unreasonably high volume of magnetic material in order to avoid core saturation.

Eq. 3.12 and Eq. 3.13 give a good initial guess about the magnetic core. Additionally, there is another popular term used by manufacturers, so-called inductance factor A_L that enables quick calculation of inductance.

$$A_L = \frac{L}{N^2} \quad (3.14)$$

Where N is turns number and A_L is inductance factor in nano Henries [nH].

Although inductance could be calculated from Eq 3.14, core saturation should be considered and avoided according to the manufacturer's recommendations. If the saturation limit is exceeded, some air gap should be inserted in the magnetic circuit of the core. A_L value can also be derived from core geometries and core properties as

$$A_L = \mu_0 \mu_e \frac{A_e}{l_e} \quad (3.15)$$

Where μ_e is effective permeability, A_e is effective area and l_e is effective length of the magnetic circuit which all of them are provided by the manufacturer.

Inserting an air gap in a core lowers effective permeability μ_e thus enables higher inductances.

$$\frac{1}{\mu_e} = \frac{1}{\mu_i} + \frac{l_g A_e}{l_e A_g \mu_0} \quad (3.16)$$

By inserting an air gap, total reluctance in the magnetic circuit increases, yielding lower magnetic flux density B at the same magnetizing force H .

Inserting an air gap into the ferrite core is not an easy task since surface quality problems or slight error in air gap length would render unacceptable results in terms of effective permeability μ_e . However, factory gapped cores are available with known

A_L and μ_e . They are also more precise and have tighter tolerances compared to ungapped counterparts. This is because the airgap dominates the magnetic circuit, makes the core structure less sensitive to mechanic assembly and material imperfections.

Another big advantage about the air gap is that it flattens the $B - H$ curve so that μ_e becomes fairly stable, yielding stable inductance. This phenomenon helps the control loop of DAB by eliminating inductance from the equation by making it nearly constant.

For all those reasons, RM12 core with a material grade of N87 from EPCOS-TDK Electronics [34] has been selected. The core has an air gap with an inductance factor $A_L = 250nH$ and effective permeability $\mu_e = 78$ compared to the ungapped variant with $A_L = 3300nH$ and $\mu_e = 1640$.

Recalling Eq. 3.12 and Eq. 3.13 respectively, we get;

$$E = \frac{1}{2} I^2 L = \frac{1}{2} \cdot (2.5)^2 \cdot 111,111 \cdot 10^{-6} \approx 347,222 \cdot 10^{-6} J \quad (3.17)$$

$$V_{e,min} = \frac{\mu_e \mu_0 E}{B_{sat}^2} = \frac{78 \cdot 4\pi \cdot 10^{-7} \cdot 347,222 \cdot 10^{-6}}{0.2^2} = 850,847 mm^3 \quad (3.18)$$

RM12 core with effective volume $V_e = 8320 mm^3$, we see that

$$V_{e,min} \ll V_e \quad (3.19)$$

which denotes that the selected core can be proceeded to further design considerations.

Recalling Eq 3.14 and solving for turns number N , we obtain

$$N = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{111,111 \cdot 10^3 [nH]}{250 [nH]}} \approx 21 Turns \quad (3.20)$$

Since the power transfer function of the DAB is highly dependent on energy storage inductance, we need to ensure its stability across all conditions including temperature and current stress. The best practice to design an inductor is to use data

sets for various conditions that are supplied by the manufacturer. EPCOS-TDK provides a very useful software for its cores.

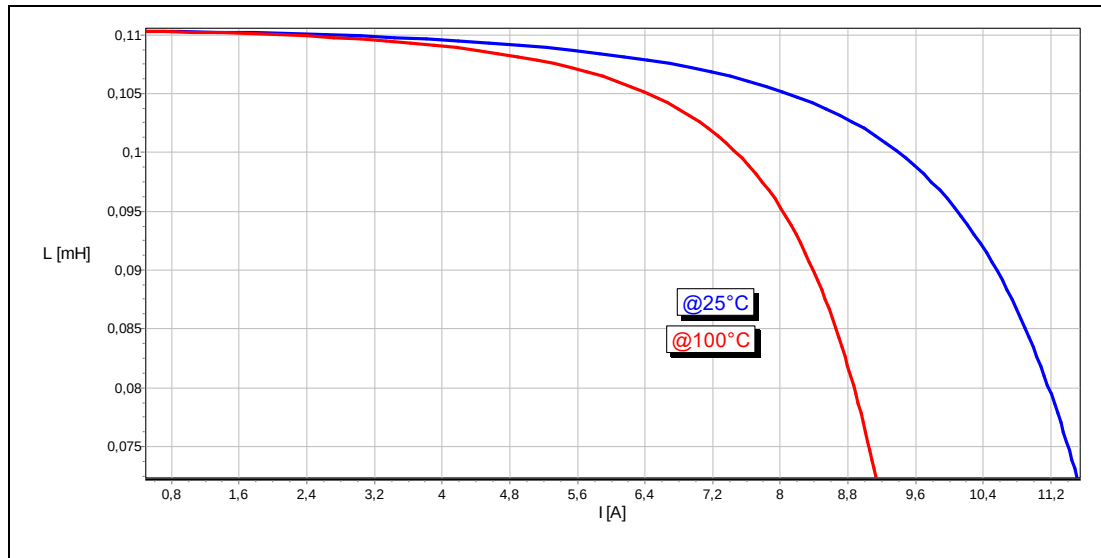


Figure 3.5: DC bias with temperature effect on DAB inductor.

Figure 3.5 shows that the designed inductor is stable over a wide range of DC bias that exceeds our RMS current rating, even at elevated temperature. However, DC bias is not expected in DAB, as can be seen in Figure 3.2 it is fully AC indeed. AC/DC winding resistance ratio of the designed inductor is depicted in Figure 3.6

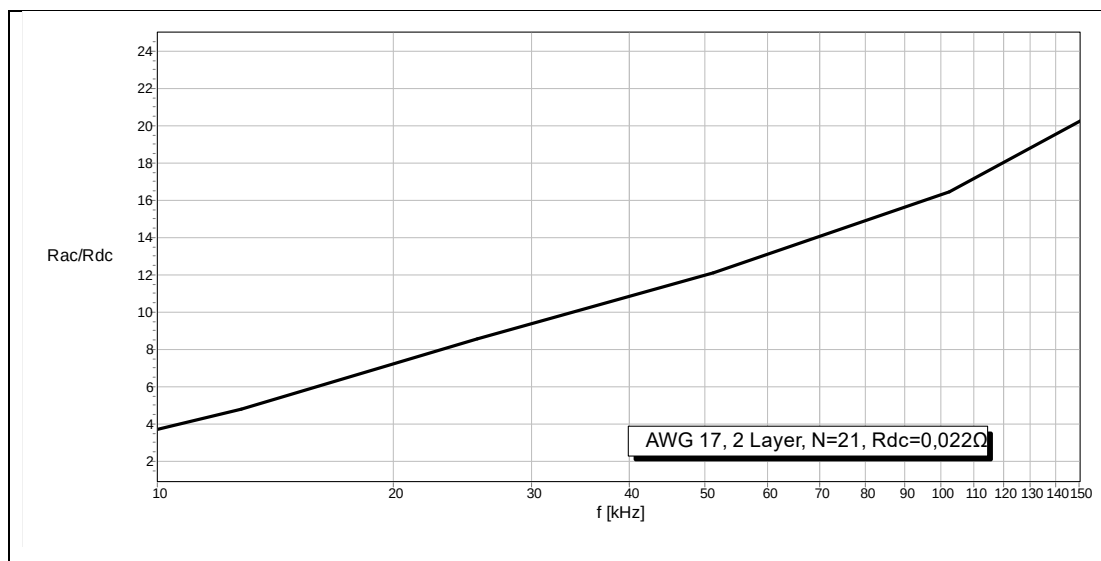


Figure 3.6: Winding resistance of DAB inductor.

Reading resistance value at 100kHz from Figure 3.6 we can calculate

$$R_{ac} = 0,022 \cdot 17 = 0,374\Omega \quad (3.21)$$

Ohmic loss can be calculated assuming that the inductor current is sinusoidal. With this assumption we get

$$I^2 R_{ac} = 2,5^2 \cdot 0,374 = 2,337W \quad (3.22)$$

Considering the power level of this design, it is a small contribution to total power loss.

3.3.2. Transformer Design

When it comes to magnetic design, the transformer design is exceptionally detailed since it is generally big and expensive thus deserves to be readily optimized. There are also multi-dimensional tradeoffs that should be considered. However, for these reasons, optimizations and in-depth calculations would be left out of our scope. Therefore, PQ5050 core from TDK [33] is selected arbitrarily. However, suitability of this core will be examined.

Using Faraday's Law of induction, turns number can easily be determined. For time-varying voltage

$$V_1(t) = N_1 \frac{d\phi}{dt} \quad (3.23)$$

By integrating both sides of the equation we obtain,

$$\int V_1(t) = \int N_1 \frac{d\phi}{dt} \quad (3.24)$$

$$DTV_1 = N_1 \phi_{p-p} \quad (3.25)$$

Since we know that $\phi = A_e B_{core}$ therefore we can replace it in the equation, and re-arranging it for N_1 , we obtain

$$N_1 = \frac{DTV_1}{N_1 A_e B_{p-p}} \quad (3.26)$$

At this point, dead time between two voltage pulses can be ignored therefore, $D = 0,5$ and $T = \frac{1}{f}$ can be inserted into equation.

$$N_1 = \frac{V_1}{2f A_e B_{p-p}} \quad (3.27)$$

In some articles and app-notes, B_{p-p} is replaced with $2 \cdot B_{peak}$ and multiplier 4 appears in the denominator is called waveform factor. That is because core manufacturers tend to provide one quadrant operation losses, thus easier to plug in the equation.

In our case, B_{p-p} is determined to be $0,2Tesla$ in order to keep losses under control. According to the manufacturer's datasheet, $A_e = 332 \cdot 10^{-6}m^2$. Using these two values and design parameters given in Table 3.1, number of turns can be calculated as

$$N_1 = \frac{V_1}{2f A_e B_{p-p}} = \frac{400}{2 \cdot 100 \cdot 10^3 \cdot 332 \cdot 10^{-6} \cdot 0,2} = 30,120Turns \quad (3.28)$$

However, fractional number of turns is not practical. Therefore it is rounded to the nearest integer of 30.

As we designed B_{p-p} to be $0,2Tesla$, the core loss curve for the selected core of PQ5050 can be seen in Figure 3.7. This figure shows that core loss behavior has a negative coefficient against temperature until $100^\circ C$ which is useful.

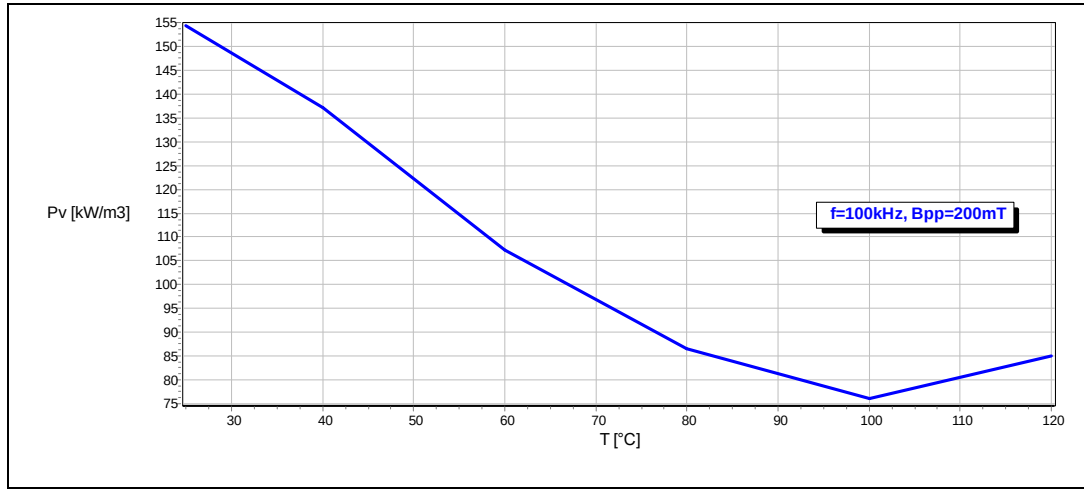


Figure 3.7: Transformer core loss of DAB.

Reading core loss parameter at 100°C and proceeding for core volume of 37270mm^3 which given in manufacturers datasheet, we get

$$\begin{aligned}
 76[\text{kW}/\text{m}^3] \cdot 37270 \cdot 10^{-9}[\text{m}^3] &= 0,002832520\text{kW} \\
 &= 2,832\text{W}
 \end{aligned}
 \tag{3.29}$$

Winding loss for the designed transformer is depicted in Figure 3.8, as a ratio of AC and DC. resistance. Since DC current is not expected, loss calculation for only AC current at designed switching frequency is enough.

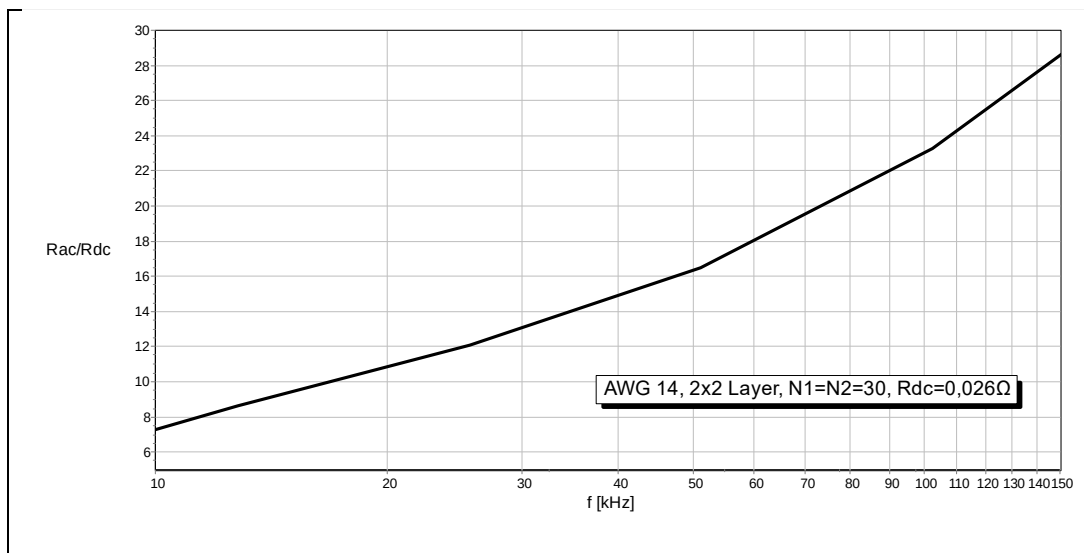


Figure 3.8: Transformer winding loss of DAB.

Reading resistance value at 100kHz from Figure 3.8 we can calculate

$$R_{ac} = 0,026 \cdot 23 = 0,598\Omega \quad (3.30)$$

We know that inductor current and transformer current are the same current since they are connected in series. It is assumed in inductor design section that the circulating current is sinusoidal. With this assumption, we calculate winding loss as

$$I^2 R_{ac} = 2,5^2 \cdot 0,598 = 3,7375W \quad (3.31)$$

This calculation is for only one side of the transformer. Therefore, total winding loss is double of calculated value since we expect the same current value at each side of the transformer. Hence, the total winding loss is

$$3,7375W \cdot 2 = 7,475W \quad (3.32)$$

Therefore winding loss along with core loss yields $7,475W + 2,832 = 10,306W$ total transformer loss. Considering $1kW$ design power, transformer loss is almost 1% of design power.

It is important to note that the DAB circuit is highly dependent on series inductance in the current path, any leakage inductance that is introduced by the HF transformer is not welcomed since the energy storage inductor is already designed. However, the leakage inductance of the transformer can be used as an energy storage inductor, even with zero additional series inductor. By using this method, the inductor in the circuit can be eliminated. Although it can provide additional benefits like cost and volume reduction of the converter, it is not easy to build and deserves whole another study. In order to keep leakage inductance lower, interleaved winding can be implemented at the construction of the transformer. Interleaved winding also helps reduce AC resistance[15].

3.3.3. Output Capacitor Design

Capacitor design for a high switching speed converter is rather easy since frequency and required capacitance is inversely proportional, hence lower capacitance is adequate. However low capacitance is beneficial in terms of the volume occupied, there are some other parameters about capacitors as important as total capacitance, such as equivalent series resistance (ESR), equivalent series inductance (ESL), dissipation factor (DF), voltage derating, etc. These factors tend to get better when multiple capacitors are used in parallel. This is especially important for high voltage, high current and high speed switching converters since capacitors need to handle high current for rather lower capacitance.

Required capacitance can be calculated, based on holding time on a specified current and maximum voltage difference. Despite this approach oversimplifies capacitor design, it is quite useful, however, some safety margins should be considered. Let's start with the instantaneous capacitor current equation

$$i = C \frac{dV}{dt} \quad (3.33)$$

Renaming parameters and solving for C we get

$$C = \frac{I_{load} t_{hold-up}}{\Delta V} \quad (3.34)$$

Since our DAB circuit operates at 100kHz, rectified current seen by the output capacitors will be 200kHz. Using the values at the table for 1% voltage change we get

$$C = \frac{I_{load} t_{hold-up}}{\Delta V} = \frac{2,5 \cdot 5 \cdot 10^{-6}}{0,01 \cdot 400} = 3,125 \mu F \quad (3.35)$$

As stated before, this calculation assumes that no load changes or disturbances will occur. When load, input, or output voltage changes are present, the controller starts to compensate it. At this point, inner control loop bandwidth has significant impact on hold-up time thus, the frequency response of the converter is critical and

directly affects capacitance that is needed. For this reason, 50 cycle holdup time is selected arbitrarily that renders required capacitance to be

$$3,125\mu F \cdot 50 = 156,25\mu F \quad (3.36)$$

Off-the-shelf capacitors are mostly standardized in terms of mounting sizes. Thus moderate changes for the total capacitance are always possible and as easy as a direct substitution. $56\mu F, 500V$ capacitor from Rubycon (500LXW56MEFR16X40) has been selected and three of them connected in parallel, resulting $168\mu F$ total capacitance. Since our design has a symmetrical power requirement, the same capacitance can also be used for the input side of the converter.

3.3.4. Closed Loop Control and Simulation

DAB converters work as power transferring converters thus provide power from one side to the other side of the converter. As the power flows through the load, voltage is created according to the power that is transferred. Our goal is to have a stable 400V output voltage within the power limit of the converter. Therefore, the designed DAB converter in previous sections has been simulated in Matlab-Simulink software. The voltage output of the converter is read and created an error signal. This error signal is then fed into PID controller. The output of the PID controller with an appropriate gain is fed into a time delay block, in order to create phase shifted gate signal from the existing original gate signal. With this configuration, it is a voltage only controller since there is no current feedback employed in the control loop. Figure 3.9 shows schematics of the control loop along with the DAB circuit itself.

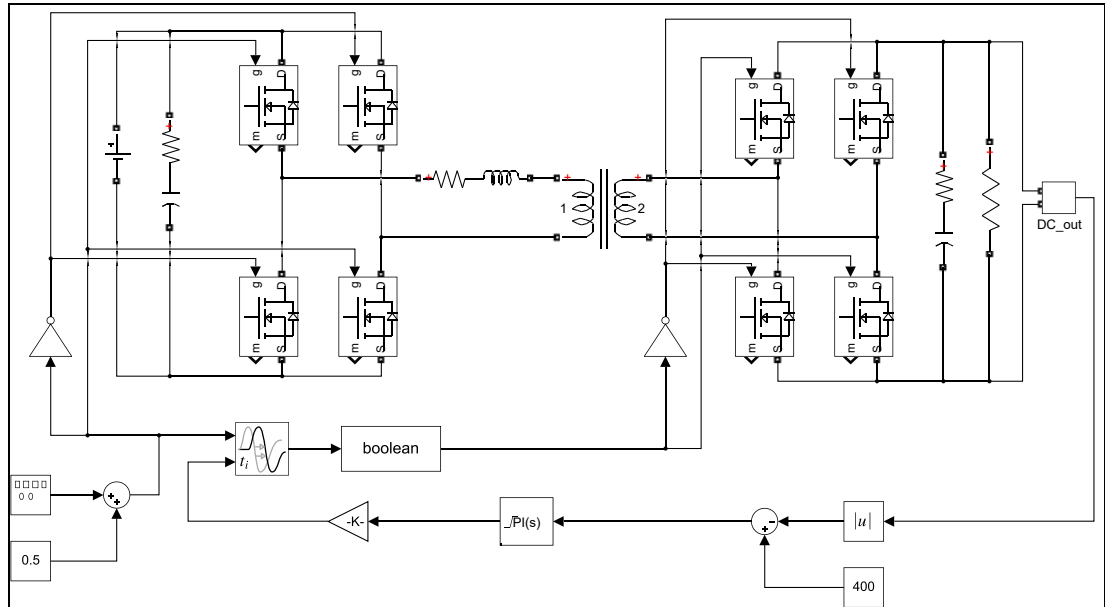


Figure 3.9: Control loop of DAB.

The circuit has been simulated for various possible situations to test its stability. One of the most important simulations is startup behavior. In Figure 3.10, startup with a load of 10% and 100% was tested.

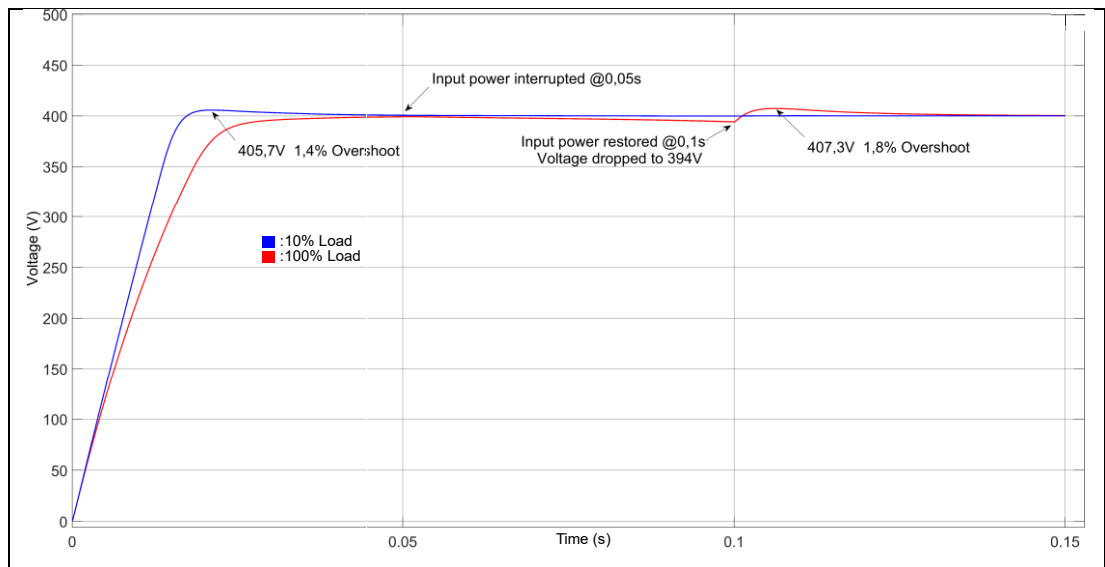


Figure 3.10: Startup and voltage interruption under load.

Under full load, the circuit startup is fairly regular and no overshoot is seen, however, there is slight overshoot under 10% load startup, which is not ideal but acceptable. Both load configurations reach steady state voltage within 50ms. In the very same

figure, there is also a voltage interruption test that starts at 0,05s and ends at 0,1s for both load levels. At 0,1s, it is very clear that the integral part of the PI compensator does need some adjustments since after 50ms voltage outage from input causes decaying input voltage on input capacitors, hence consume maximum phase shift available. This is apparent in the output voltage curve of 100% load. Integral part cumulates error signal over time and since the interval of voltage interruption is fairly long compared to switching period, overshoot of 1,8% occurs which is also not ideal but acceptable.

Uncertainty of load behavior is always present therefore load step might be a good test for our circuit. High to low and low to high load step for 50% and 10% loads are shown in Figure 3.11.

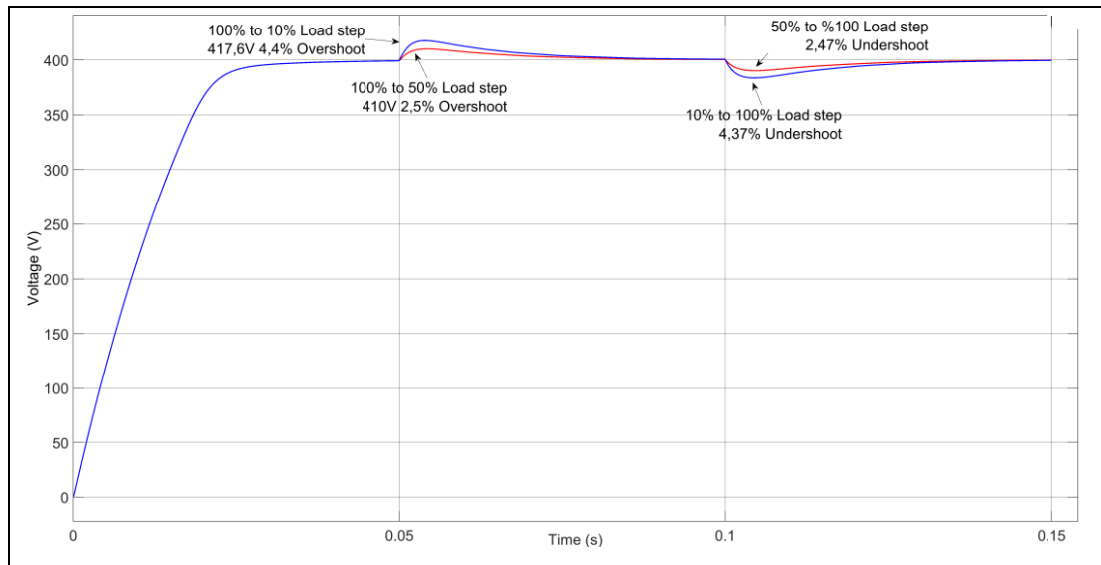


Figure 3.11: Load step from high to low and low to high.

The system reaches steady state before the first load step of low to high load step at 0,05s. As the load drops immediately, PI compensator begins to rewind the phase shift parameter. As can be seen in the waveform, a bigger step causes a bigger overshoot. The second load step occurs at 0,1s from low to high load. Similarly, the control plant needs some time to recover the system whilst experiencing undershoot at the output voltage.

Finally, the last simulation is AC superposed input voltage simulation. Since the PFC converter output will feed the input of the DAB circuit, the mains frequency ripple might be seen at the output of the PFC converter. Since the PFC converter rectifies

mains input voltage, double frequency of 50Hz appears at the output voltage. Therefore, 100Hz sinus is superposed to input voltage aiming to mimic input ripple of 400VDC. It is depicted in Figure 3.12 where the ripple is coupled right after 0,1s

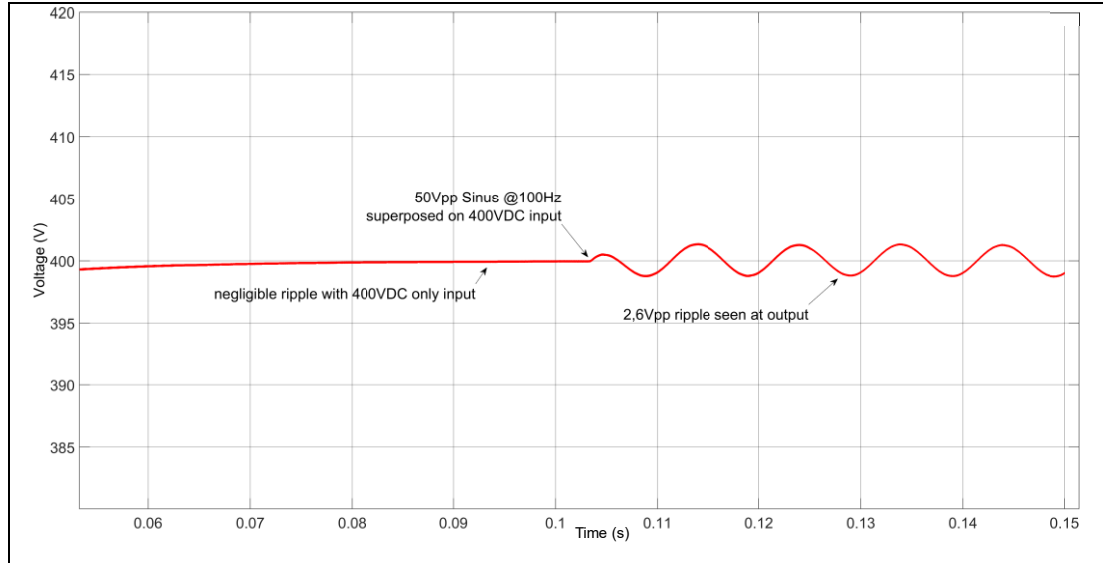


Figure 3.12: Output voltage when 50Vpp is superposed to the input voltage.

Arbitrarily decided 50Vpp AC coupling on input voltage is somewhat exaggerated, however, the control loop compensates it very well with a damping value of roughly -25dB

As a result, the designed DAB controller works well with minor flaws such as overshoot and undershoot issues. If a particular application needs stricter output voltage compensation, there are possibilities to tweak the PI plant. In this study, PI parameters are empirically decided to be $PI_{proportional} = 0,003$ and $PI_{integral} = 0,25$ which gives an overall performance. There are tradeoffs when tuning parameters such as settling time, transient response, steady-state error, and bandwidth etc. Final tuning should be performed according to end product, and performance expectations.

4. PFC AC-DC CONVERTER

4.1. Overview

When pulling current from AC line, current may not be necessarily in phase with the line voltage. This behavior causes some unwanted, irregular current spikes and reactive power consumption which is bad for electric distribution. Thus, devices with AC line input must comply with international regulations such as EN 61000-3-2.

PFC converters ensure that the system is within allowed limits. It synchronizes the input current of the system to the input voltage. It is done by either passive or active. Passive PFC means that the switching devices, mostly transistors, are not involved in the design. Therefore, a control loop is not needed. However active PFC contains at least one switching device and an inherent control loop. It controls the input current by chopping and shaping it, as it is in phase with the input voltage. By doing that, current conduction time is extended, therefore RMS current spikes are avoided, compared to non-corrected power factor. It also eases stresses on active and passive components.

Conventional PFC converters generally have a rectifier stage and a boost stage. When the rectifier stage is made of diodes, it is called bridged PFC. Bridge ensures positive voltage is supplied to boost converter for each half cycle of the mains input. However, since diodes are not controllable, passive diode bridge prevents bidirectional power flow. At this point, diodes can be replaced with transistors, in our case they are MOSFETs. MOSFETs can enable bidirectional power flow thanks to their controllable nature. Since no diode is involved, transistorized PFC converters are called bridgeless converters. The following boost stage is responsible for controlling the input current shape while performing boost operation to create stable DC output voltage. Boost stage shapes input current that the fundamental frequency of the input current matches and in phase with the mains voltage.

PFC converters can be operated in continuous conduction mode (CCM), critical conduction mode (CRM), or discontinuous conduction mode (DCM). In CCM, as the name implies, the converter ensures that the inductor current never reaches zero. This eases stress on the inductor and switching transistor. However, this pushes the system into hard switching. In DCM and CRM, boost inductor current falls to zero, involving

a much larger current delta as well as higher peak currents, in order to keep RMS current high enough. High current spikes and large current delta puts extra stress on the inductor and switching transistor considering RMS output current. Since current can reach zero for every switching cycle, switches can perform ZVS and zero current switching (ZCS) which lowers switching losses significantly.

High voltage high power PFC converters tend to implement CCM converters. Since high voltage and high currents are already involved, DCM and CRM can put extra stress on the inductor and switching transistors that would render the design impractical.

Basic bridgeless PFC converters have two high speed transistors and two freewheeling diodes. At this point, it is just two separate boost converter for positive and negative half cycles of the AC mains input voltage. In order to get bidirectional current flow, freewheeling diodes must be replaced with transistors. Totem pole bridgeless PFC has four switches, two for high speed boost switches working in complementary sequence, other two for rectification. High speed leg of the converter is called the totem leg and the other leg is called the rectification leg.

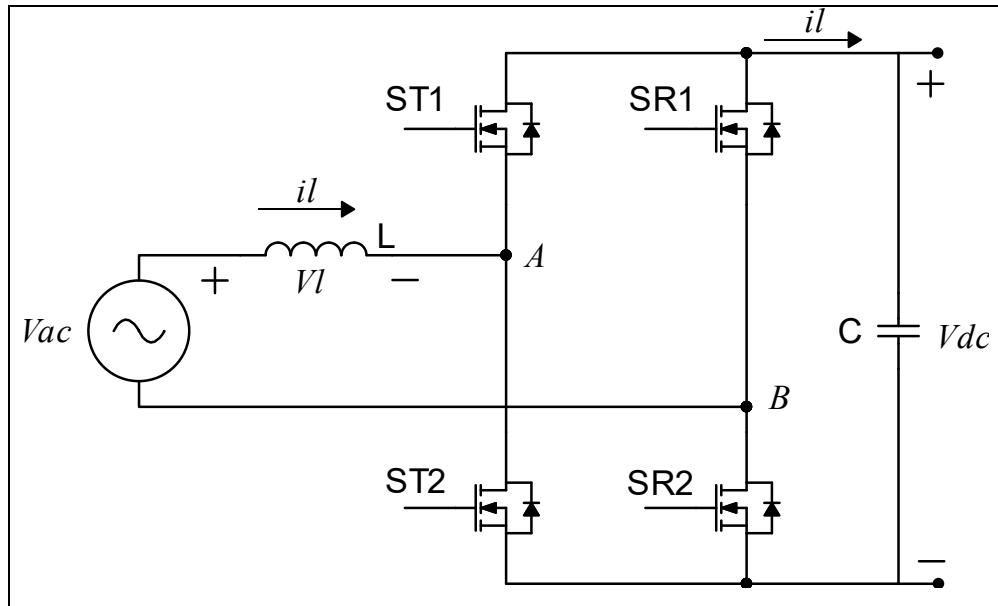


Figure 4.1: Basic schematic of Totem Pole bidirectional PFC converter.

4.2. Selected PFC Method: Totem Pole Bridgeless PFC

In this method, power factor correction is done by two high speed switches, responsible for correcting inbound current in a complementary fashion whereas the other two transistors are slow and for conducting current at line frequency while rectifying it. The current loop for positive and negative half cycles can be seen in Figure 4.2 [30].

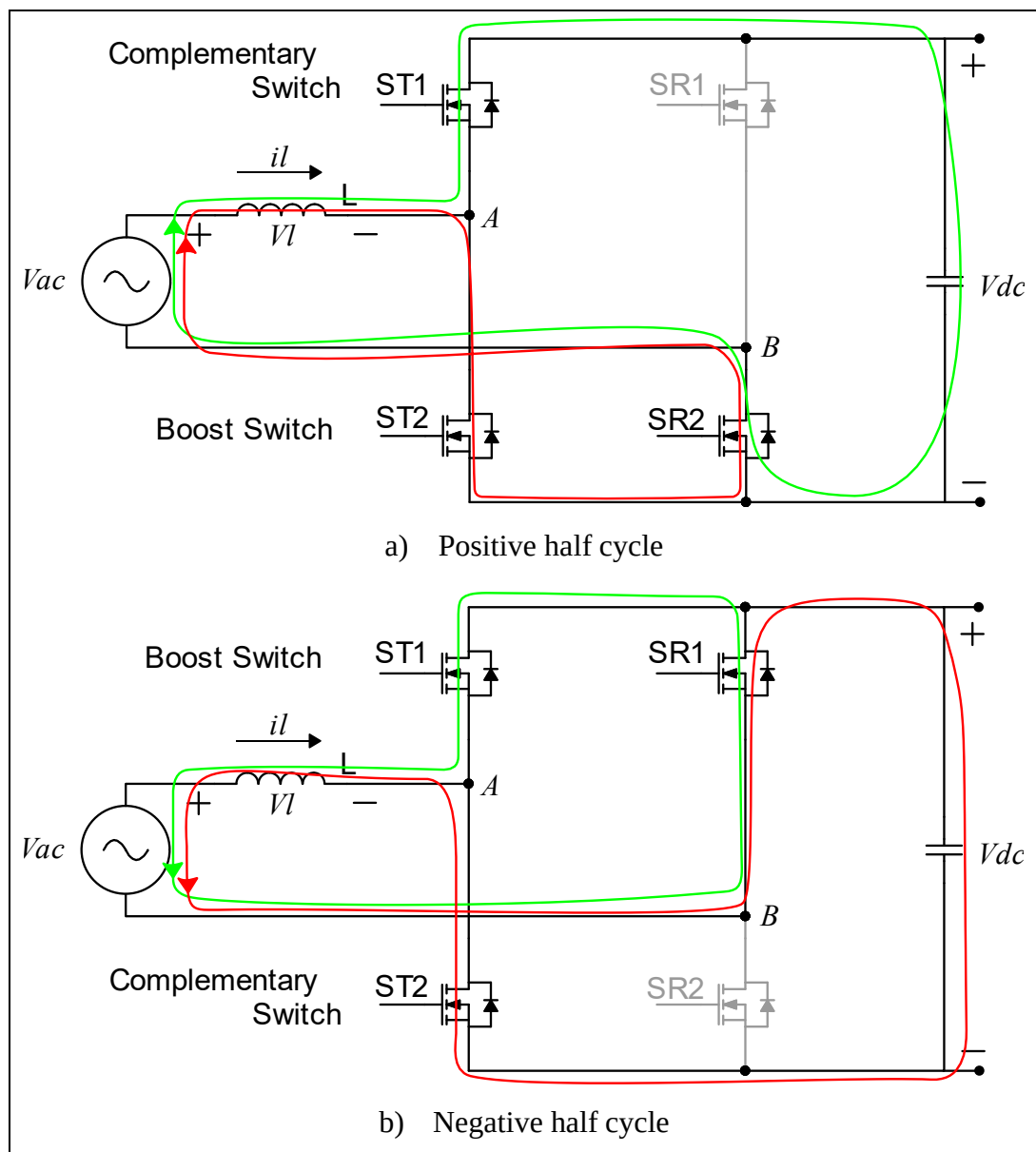


Figure 4.2: Current loop for Totem Pole PFC Converter during one grid cycle.

As this study seeks for bidirectional AC-DC converter and plans to integrate it in OBC or home batteries, it must be extremely efficient and must be compliant with various standards and restrictions. Due to these challenging design constraints. Bidirectional totem-pole PFC boost converter topology is selected. For both G2V and V2G operations are explained and equations are derived in order to determine core elements, such as boost inductor and switching transistors.

4.2.1. Charging (G2V) Mode

Charging mode, grid to vehicle (G2V) mode, positive current mode are equivalent terms that tell us the converter draws power from the grid. When pulling current from the grid, the current should be in phase with the grid voltage. Hence, the load seen by the grid becomes like a resistive load. Therefore, reactive power demand from the grid decreases, and apparent power and real power drawn from the grid would be fairly close to each other as well.

When positive half cycle from the grid appears on the converter, transistor ST2 acts as a boost switch and charges the boost inductor by turning on during duty time (D) whereas ST1 is turned off as it blocks back current from the output capacitor, whilst on the rectifier leg, transistor SR1 is turned off and transistor SR2 is turned on in order to enable positive current through output capacitor C of the PFC converter and the load. However, during negative grid voltage, totem leg switches swap around their roles and similarly, rectifier leg switches also swap around their roles. When negative half cycle from the grid appears on the converter, transistor ST1 acts as a boost switch and charges the boost inductor by turning on during duty time (D) whereas ST2 is turned off as it blocks back current from the output capacitor, whilst on the rectifier leg, transistor SR2 is turned off and transistor SR1 is turned on in order to enable positive current through output capacitor C of the PFC converter and the load.

Boost operation is done by implementing simple boost mechanics. Boost switch is driven by a PWM that is modulated by boost algorithms. Considering slow change on input voltage compared to the switching frequency of the PFC, the input voltage can be estimated as constant over one switching period.

4.2.2. Inductor Design

The inductor in totem-pole PFC topology determines the current slopes of the system. When performing G2V operation, it acts as a boost inductor since even peak voltage of 230Vrms mains voltage is not enough for 400VDC input of DAB converter. Thus, it needs to be boosted. Although it is named boost inductor, it is also a buck inductor when the converter operates V2G mode. However, G2V equations derived before will be used to determine a minimum value for the inductor.

We know that maximum current ripple is

$$\Delta i_L = \frac{V_{DC}D(1-D)}{fL} \quad (4.1)$$

It is clear that Δi_L is maximum at duty cycle $D = 0,5$

Our system is designed for 1KW output for 230Vrms input voltage, the input current is 4,35Arms. Assuming that the input current is ideal sinusoidal therefore peak input current is $4,35 \cdot \sqrt{2} = 6,15A$.

With 20% current ripple parameter,

$$\Delta i_L = 6,15 \cdot 0,2 = 1,23A \quad (4.2)$$

Plugging every parameter in Eq. 4.1 and solving for L we obtain

$$L = \frac{V_{DC}D(1-D)}{f\Delta i_L} = \frac{400 \cdot 0,5 \cdot (1-0,5)}{100 \cdot 10^3 \cdot 1,23} \approx 813\mu H \quad (4.3)$$

It is greater than the DAB converter inductor, in terms of both current and inductance value, that is designed in previous sections. Therefore, a bigger core RM14 from TDK-EPCOS [35] has been selected. Since ferrites have fairly high permeability and low magnetic saturation property, an air gap should be used for the required inductance at the required current flow. Thus, effective permeability is lowered.

RM14 core with $A_L = 160nH$ is examined since it is an off-the-shelf product. Recalling Equation 3.4 for required turns ratio, we obtain,

$$N = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{813 \cdot 10^3 [nH]}{160 [nH]}} \approx 71,282 Turns \quad (4.4)$$

Since fractional winding is not practical, it is rounded to the nearest greater number of 72. However, DC bias is disregarded at this point, thus final decision about turns number must be corrected according to the manufacturer's data.

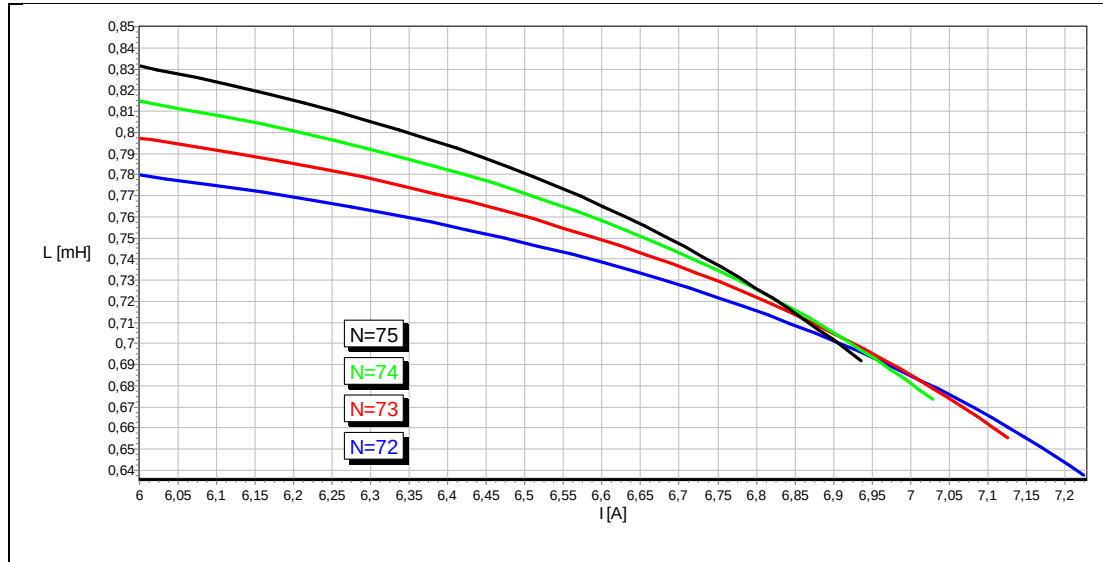


Figure 4.3: DC bias comparison of various turns of PFC inductor.

In Figure 4.3, the inductance value against DC bias current is depicted for various turns ratio. It can be seen that higher turns ratio yields higher inductance until core flux density exceeded. After that point, the inductance value falls sharply and cannot keep desired inductance value. This effect can also be seen in Figure 4.4.

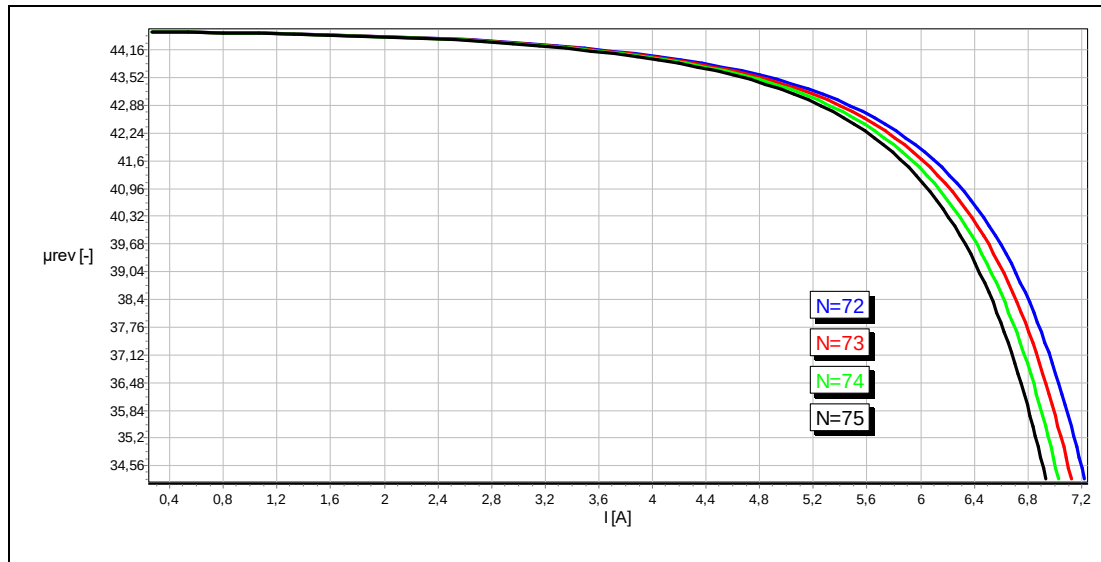


Figure 4.4: Reversible permeability for various turns of PFC inductor.

Higher turns number combined with high DC current degrades reversible permeability quicker compared to lower turns number. With this regard, turns number is decided to be 72 since it provides wider operational current capability despite its lower inductance.

Since we calculated DC and AC part of the inductor current, we can calculate winding losses of the inductor. The ratio of winding resistance is depicted in Figure 4.5.

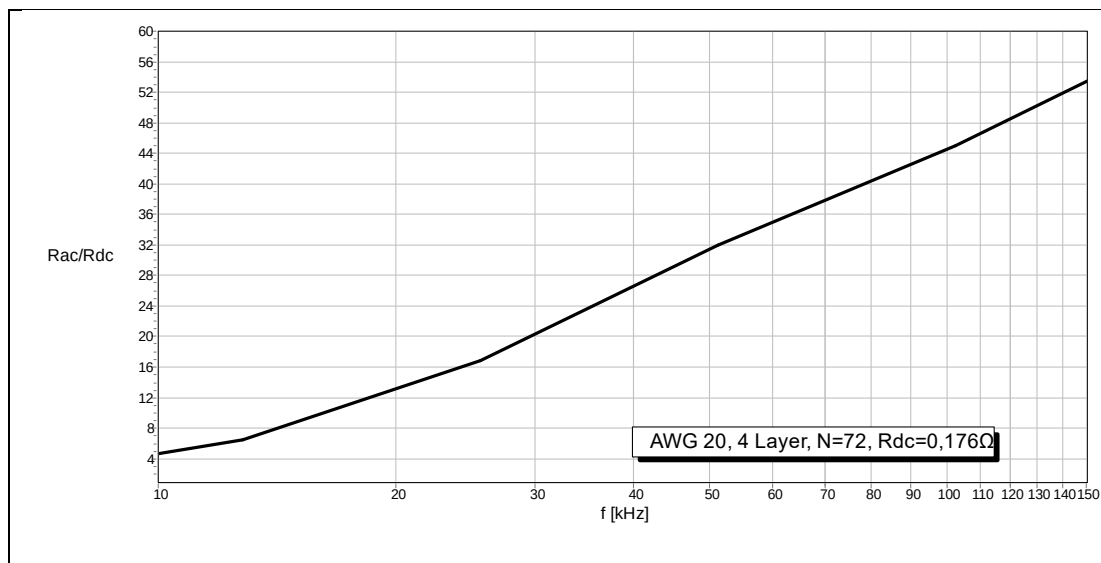


Figure 4.5: Winding resistance of PFC inductor.

Knowing that $R_{dc} = 0,176\Omega$ thus AC resistance can be calculated as

$$R_{ac} = 45 \cdot 0,176 = 7,92\Omega \quad (4.5)$$

Since PFC converter supplies DC current as well as superposed AC current. Therefore, the major contribution to winding loss comes from the DC part of the inductor current. To calculate DC winding loss, we can write

$$I_{RMS}^2 R_{dc} = 4,35^2 \cdot 0,176 = 3,330W \quad (4.6)$$

AC winding loss can also be calculated like DC winding loss

$$\Delta i_L^2 R_{ac} = 1,23^2 \cdot 7,92 = 11,982W \quad (4.7)$$

This loss might sound big at a glance however, this loss is not static. This is the highest AC winding loss when the highest AC current occurs at $D = 0,5$. Usually, AC current is much lower throughout one switching cycle. Therefore, the total winding loss is higher than DC winding loss but doesn't reach anywhere near AC and DC winding loss combined.

4.2.3. Output Capacitor Design

The output of the PFC converter needs to be smoothed out in order to provide a good interface between the DAB converter and the PFC converter. Considering that the input current of the PFC converter is sinusoidal thus output current is sinusoidal whereas it is rectified. Since it is rectified, the fundamental frequency of the output current is 100Hz, double of the grid voltage frequency 50Hz. This fundamental frequency must be smoothed in terms of voltage. To begin with capacitor sizing, the instantaneous current equation for a capacitor is given as

$$i = C \frac{dV}{dt} \quad (4.7)$$

Rearranging it to calculate C , and integrating both sides of the equation, we obtain

$$C = \frac{1}{\Delta V} \int i(t) dt \quad (4.8)$$

Since output current $i(t)$ reaches its maximum value at half period, integration over half period and changing from time domain t to angular frequency ω we obtain

$$C = \frac{2I}{\omega \Delta V} \quad (4.9)$$

In order to find a good balance between output voltage ripple and output capacitance, the ripple voltage ΔV is decided to be 5% resulting in 20V peak to peak voltage ripple. This value can be adjusted according to the following DC-DC converter performance. A better control strategy on DC-DC (DAB) converter can be highly beneficial thus helps to lower the output capacitance of the PFC converter. This also enables higher volumetric density as well as reduces total cost.

Inserting the values, the capacitance is calculated as

$$\begin{aligned} C &= \frac{2I}{\omega \Delta V} = \frac{2I}{2\pi f \Delta V} = \frac{2 \cdot 6,15}{2 \cdot \pi \cdot 100 \cdot 20V} \\ &= 978,802 \mu F \end{aligned} \quad (4.10)$$

150 μF , 500V capacitor from KEMET (ESG157M500AQ5AA) has been selected for this study, and seven of them connected in parallel, resulting in 1050 μF total capacitance

4.2.4. Closed Loop Control and Simulation

As explained earlier, the PFC circuit is basically a regulating interface between load and AC mains input that shapes input current thus it looks like the input voltage waveform. Therefore the load seen by the input voltage is like a resistive load. To obtain this behavior, a control loop should be implemented.

The Totem Pole PFC circuit setup is shown in Figure 4.6. There are two high speed switching MOSFETs controlled with signals named ST1 and ST2 that act as a boost converter. For each cycle of mains input, they swap their roles as explained earlier. This leg of the bridge is called totem pole leg. There are another two switching MOSFETs alongside the totem leg. This leg of the bridge rectifies line voltage with a control signal named SR1 and SR2 thus switches at twice the input line frequency. Therefore these switches are slow compared to totem leg.

MOSFETs have an inherent body diode as shown in Figure 4.6. Therefore enormous amount of current can flow without a soft start feature. There is no such mechanism in the basic Totem Pole PFC circuit that limits input current at start-up, hence two additional single pole single throw (SPST) ideal switches are added to the circuit. These SPST switches ensure limited current flow through the circuit by adding series resistance to the mains input. When the control loop starts compensating, the run signal bypasses series resistance to reduce loss on the resistance. This type of start-up inrush current limiting is adopted by manufacturers as they add a series NTC thermistor element with a parallel bypass mechanical relay[16].

The input grid voltage is read with V_s signal and the output of the PFC is read with V_o signal. Additionally, current flow through the inductor is read with i_L signal to be fed to the control loop.

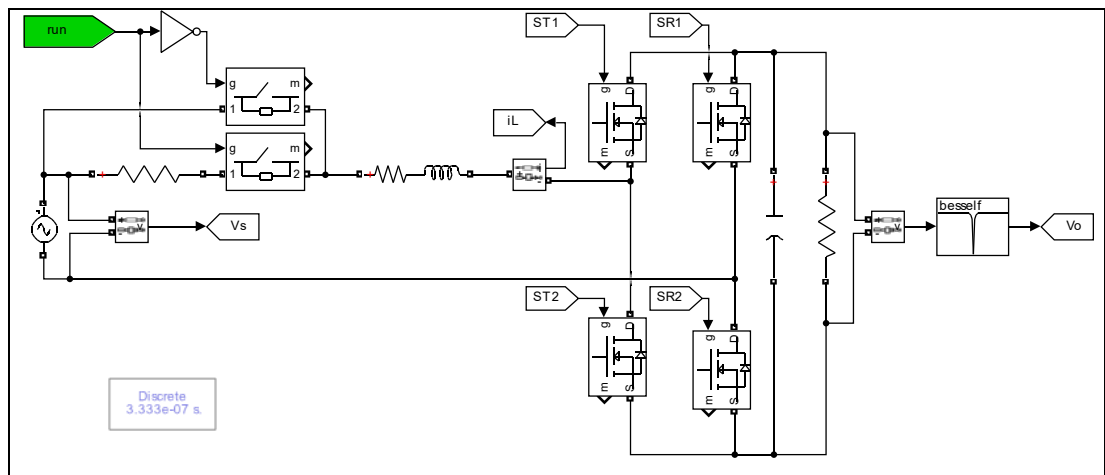


Figure 4.6: Simulated bidirectional Totem Pole PFC circuit.

A control loop is designed in Matlab Simulink environment with built-in building blocks shown in Figure 4.6. There are two control loops that are responsible

for two different parameters, voltage loop, and current loop. Both voltage and current control loop employ separate PI controllers with different coefficients.

The main control loop is the current control loop since the main purpose of the PFC circuit is to maintain a well-shaped input current with minimal Total Harmonic Distortion (THD) as well as a unity power factor. Therefore, the current PI controller is faster than the voltage loop, hence has big coefficients, whereas the voltage PI controller is slow and has small coefficients. Additionally, there is a band stop filter before output voltage signal that filters out around 100Hz mains ripple. This is beneficial since few volts of ripple at 100Hz is expected. Without this filter, a small error signal is created at every mains cycle and injected in the control loop, resulting in an unnecessary disturbance at the overall control loop.

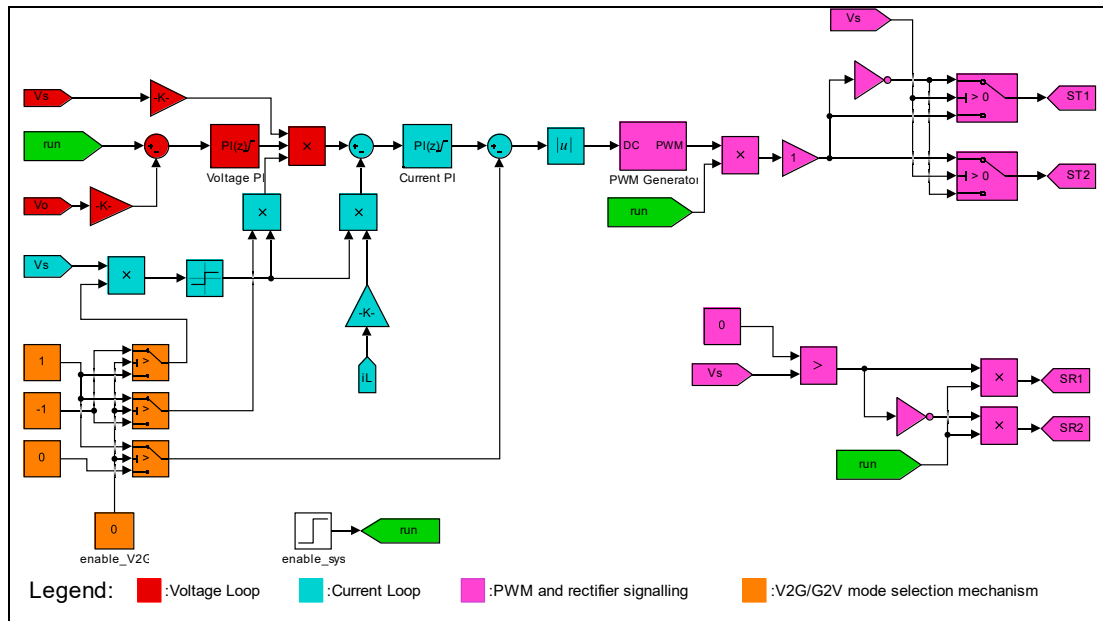


Figure 4.7: Control loop of simulated bidirectional Totem Pole PFC circuit.

In order to start the control loop, an enable signal is implemented. This enable signal triggers run signal distributed to various system inputs as well as inrush current limiter mechanism at $T=0,02s$.

After run signal, the grid voltage is multiplied by a gain block and rectified by taking the absolute value of it. This value is then multiplied by voltage loop compensator output. However, when the system arrives to steady state, no perturbation is introduced by the voltage control loop. As a result, this creates a basis for the current control loop reference signal. To create an error signal for the current PI block, the

inductor current is multiplied by the polarity of the grid signal then scaled with gain block. The resulting signal is subtracted from the reference signal and fed to the current PI controller. Finally, the output of the current PI controller is fed to the PWM generator. The output of the PWM generator is distributed to totem leg MOSFETs according to their complementary role determined by the grid voltage polarity.

In addition to totem leg, rectifier leg control signals are derived from grid voltage polarity without any compensator.

The circuit showed in Figure 4.6 with the control loop shown in Figure 4.7 has been simulated at full load. Line input voltage and input current are given on the same graph and output voltage is given below it.

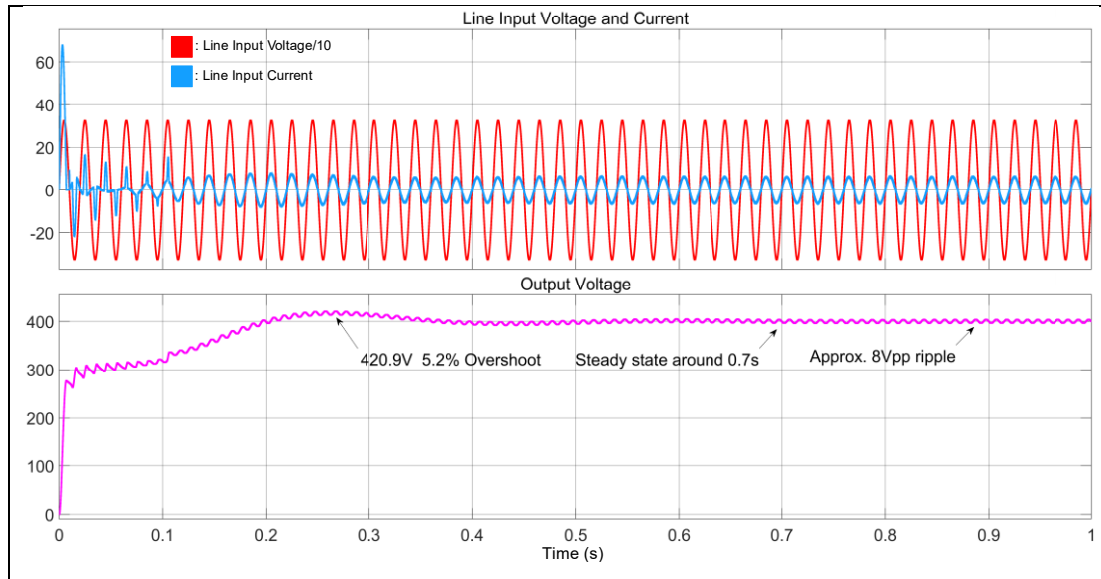


Figure 4.8: Input voltage, input current, and output voltage of the simulated bidirectional PFC circuit in G2V operation.

Input current peaked to over 60A in the first half cycle of the grid input voltage, which can easily be handled by most of the power MOSFET body diodes in the market. Within few cycles, input current starts to resemble grid input voltage. Output voltage overshoots 5,2% reaching 420,9V due to integral part of the voltage PI compensator. The integral part of the voltage PI compensator is necessary since it ensures zero steady state error. A very low or zero integral part would significantly increase transient duration when load changes occur including start up.

At 0,7s, output voltage reaches steady state with nearly 8Vpp voltage ripple. Steady state zoomed in waveforms are depicted in Figure 4.9.

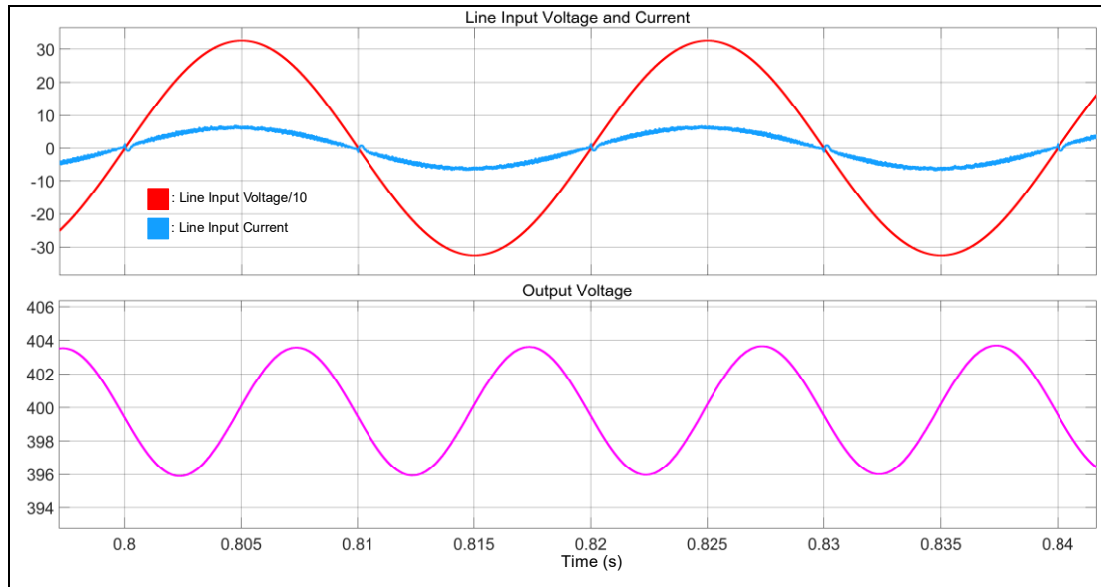


Figure 4.9: Input voltage, input current, and output voltage of the simulated bidirectional PFC circuit at steady state in G2V operation.

Steady state waveform is used to calculate harmonics produced by the input current. This is an important measure of the PFC converter, showing how good input current is shaped. Fast Fourier Transform (FFT) of the windowed waveform showed in Figure 4.10. This FFT resulted in 7,9% *THD*, depicted in Figure 4.11 with $\phi = 3,4^\circ$ phase difference at the fundamental frequency.

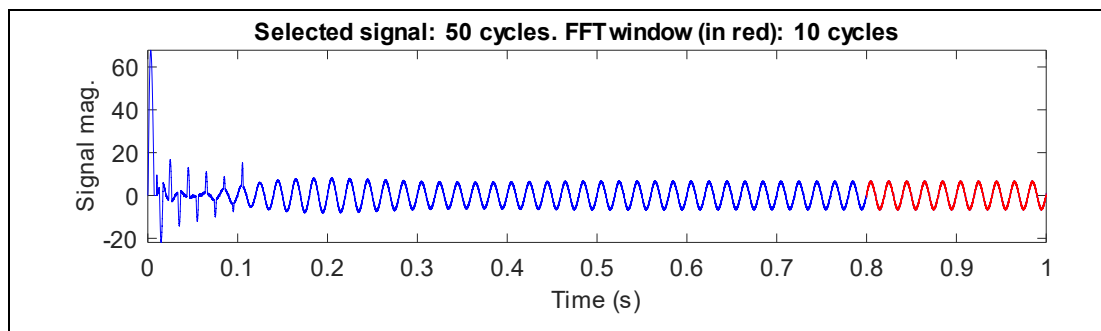


Figure 4.10: FFT window of the input current at steady state in G2V operation.

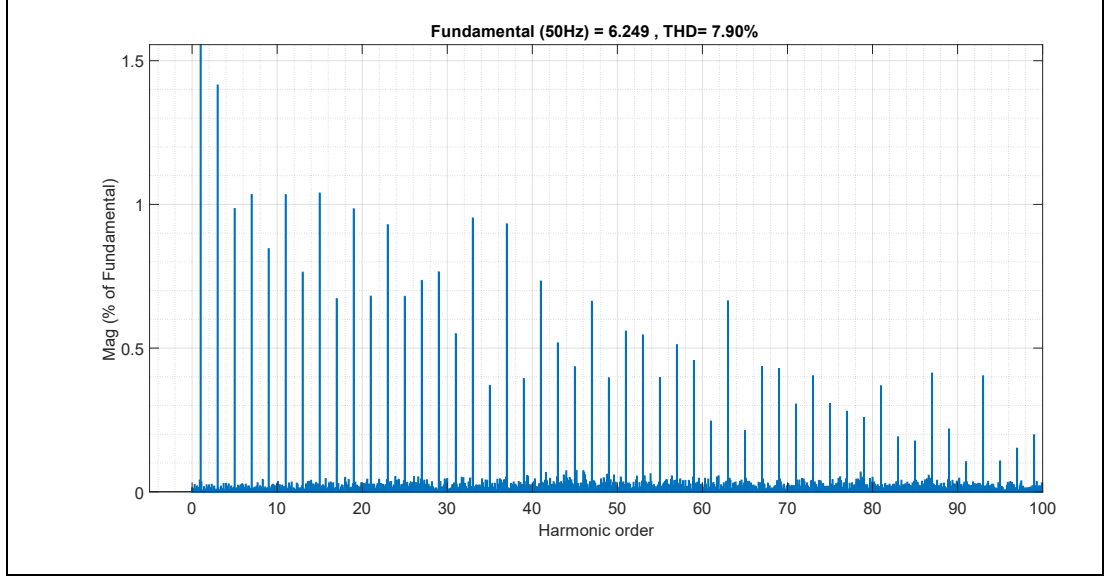


Figure 4.11: Harmonics of the input current at steady state in G2V operation.

This phase difference can be used to calculate the displacement power factor (DPF), which is power factor in linear circuits.

$$DPF = \cos(\phi) = 0,998 \quad (4.11)$$

Since phase difference and THD is known, power factor can easily be calculated as stated in [17, ch: 3-2-4-5, eq 3-45]

$$pf = \frac{1}{\sqrt{1 + THD^2}} DPF = 0,995 \quad (4.12)$$

Even though THD is not ideal, the calculated power factor is certainly much better. THD can be improved with well-known techniques when actual hardware is developed. This is discussed in the future work section.

To push the control loop in V2G mode, an input parameter *enable_V2G* along with 3 switches are employed as depicted in Figure 4.7. When this parameter is set to 1, the grid voltage measurement V_s and inductor current measurement i_L is inverted because current is supplied to the grid, rather than drawn from the grid. To compensate this, output of the current PI controller is adjusted to perform buck operation, since it is in boost mode in G2V operation.

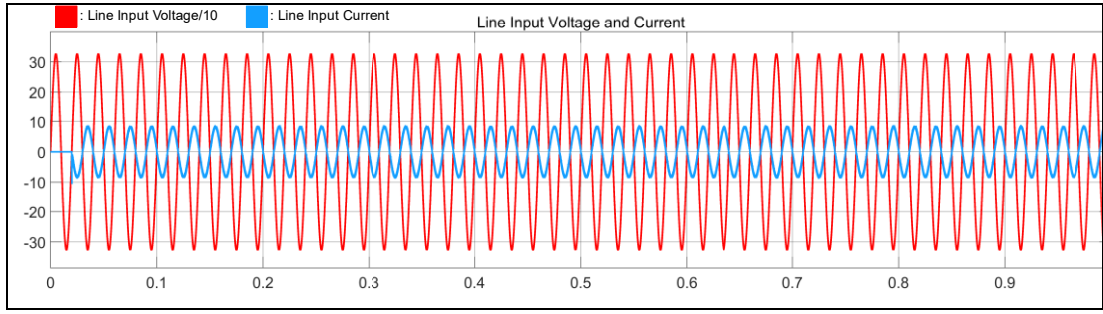


Figure 4.12: Input voltage and input current of the simulated bidirectional PFC circuit in V2G operation.

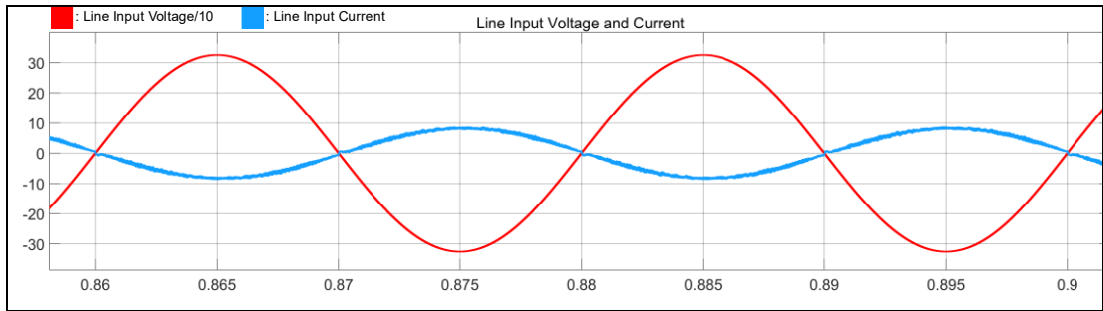


Figure 4.13: Input voltage and input current of the simulated bidirectional PFC circuit at steady state in V2G operation.

In V2G mode, the input current and the grid voltage are out of phase since the power flows to the grid as depicted in Figure 4.8.

Steady state waveform is used to calculate harmonics produced by the input current, as done for simulation of G2V operation. This FFT resulted in 5,09% *THD*, depicted in Figure 4.15 with $\phi = 3^\circ$ phase difference at the fundamental frequency.

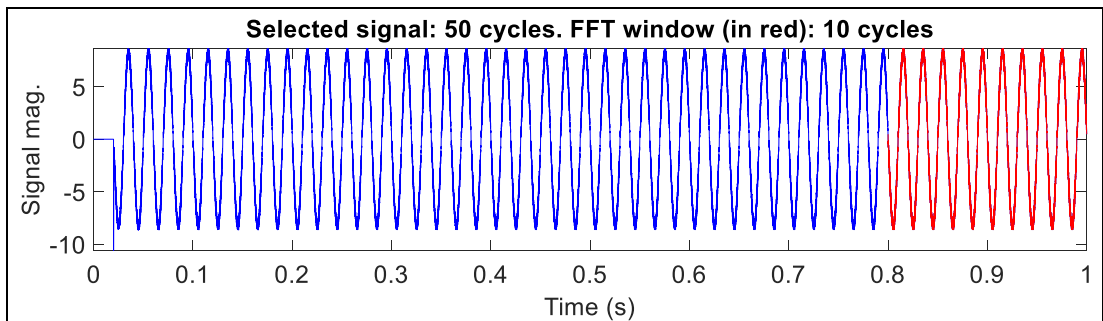


Figure 4.14: FFT window of the input current at steady state in V2G operation.

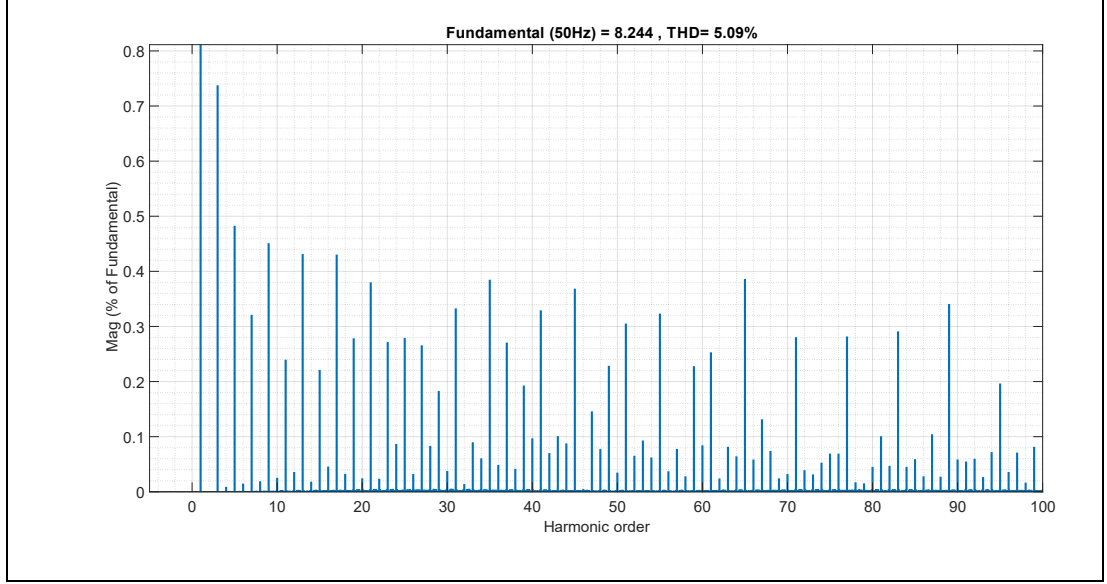


Figure 4.15: Harmonics of the output current at steady state in V2G operation.

Recalling equations in 4.11 and 4.12 to calculate DPF and pf for V2G operation, we get

$$DPF = \cos(\phi) = 0,998 \quad (4.13)$$

$$pf = \frac{1}{\sqrt{1 + THD^2}} DPF = 0,996 \quad (4.14)$$

PI compensation network has a very high influence on performance metrics of the PFC converter, compared to DAB control. There are two PI compensators in the design, one is a voltage compensator and the other is a current compensator. Current PI constants are $PI_{current,proportional} = 0,21$ and $PI_{current,integral} = 1800,5$. Voltage PI constants are $PI_{voltage,proportional} = 1$ and $PI_{voltage,integral} = 100$. These constants are refined with empirical methods to have the best power factor and lowest harmonics. There are other metrics such as settling time, overshoot, bandwidth etc. to be considered. As noted in DAB section, these parameters should be tuned for desired performance of the end product.

5. CONCLUSIONS

There are different techniques and topologies for an OBC however, few of them are capable of delivering bidirectional current flow. Bidirectional OBC devices are thought to be future OBC standards because of forecasted increasing demand for charging energy. Market trend for bidirectional OBC is two section charger, a PFC circuit for grid frontend followed by a DC-DC converter for isolation and charging profile purposes. In this study, Bidirectional Totem Pole PFC for grid frontend PFC section and Dual Active Bridge (DAB) for DC-DC section have been examined.

Topology waveforms, inductor design, transformer design, and capacitor design have been completed for DAB circuit from readily available off the shelf parts. Additionally, core and copper losses are computed for the designed inductor and transformer. Power transfer equation is the most important observation considering DAB topology hence, it is derived from scratch. Equations are derived step by step basis to design reactive elements of the DAB. This approach is adopted to be beneficial for different design goals as well as providing overall design experience. Therefore, different power, voltage or even switching frequency levels are aimed to be possible by following this study. The designed circuit is simulated in Simulink environment for various operating conditions. Control algorithms are provided, and corresponding results are shown.

PFC circuit is the grid end of the system hence designed to be sound as much as possible. Inductor and output capacitor are calculated and designed using off the shelf parts. Since the PFC inductor is expected to deliver high amount of low frequency (50 Hz) current, DC bias for the designed inductor is discussed and loss characteristics have been examined. Control algorithm for Bidirectional Totem Pole PFC topology is moderately complicated. Therefore, a detailed control scheme has been shown. This control algorithm is then simulated for various load conditions. As the name implies, this is a power factor correction circuit, therefore, current harmonics and power factor are obtained by simulation for both G2V and V2G operation.

6. FUTURE WORK

Even though this study is expected to use SiC FETs, simulated circuits are designed with nearly ideal MOSFETs along with a nearly ideal body diode. In order to simulate as close as possible to a real circuit, switches need to be modeled extensively. GaN FETs are very promising switches and might provide additional efficiency for both the PFC and the DAB section of this thesis. In this regard, designed two section OBC deserves to be simulated as a whole, with a charging algorithm implemented.

In Bidirectional Totem Pole PFC design, 230VAC is chosen to be our study case however, 110VAC grid is used in some high populated countries. Therefore, 110VAC compatibility should be studied. Power factor is calculated to be very good but THD should be improved. To improve THD, input EMI filters might be implemented.

In DAB design, leakage inductance introduced by HF transformer is neglected. The inductor is a very important parameter for a DAB design since it determines maximum power flow at a certain phase shift. Excessive inductance cripples the ability to transfer power between two ends of the DAB. This is crucial because leakage inductance is highly beneficial in DAB since enables us to design smaller discrete inductor or even eliminates it. Therefore the transformer design deserves whole another study.

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Ahmet Faruk Kantepe has born in 1994. He received his bachelor's degree in electronic engineering from Gebze Technical University, Kocaeli, Turkey in 2017. He is expecting his master of science degree with this thesis. He worked as a hardware design engineer in Antsis Elektronik, and recently, started to work on mild hybrid vehicles in AVL Research and Engineering Turkey. His key interests include high power conversion, wide bandgap transistors, and highly integrated DC-DC converters.