

T.R.
GEBZE TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

**DESIGN OF PHASE-LOCKED LOOP BASED RADIO FREQUENCY
SYNTHESIZER**

OSMAN YURDAKUL
A THESIS SUBMITTED FOR THE DEGREE OF
MASTER OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

GEBZE
2019

T.R.
GEBZE TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

**DESIGN OF PHASE-LOCKED LOOP BASED
RADIO FREQUENCY SYNTHESIZER**

OSMAN YURDAKUL
A THESIS SUBMITTED FOR THE DEGREE OF
MASTER OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

THESIS SUPERVISOR
ASSIST. PROF. DR. ÖNDER ŞUVAK

GEBZE

2019

T.C.
GEBZE TEKNİK ÜNİVERSİTESİ
FEN BİLİMLERİ ENSTİTÜSÜ

FAZ-KİLİTLEMELİ ÇEVİRİM TABANLI
RADYO FREKANS SENTEZLEYİCİ
TASARIMI

OSMAN YURDAKUL
YÜKSEK LİSANS TEZİ
ELEKTRONİK MÜHENDİSLİĞİ ANABİLİM DALI

DANIŞMANI
DR. ÖĞR. ÜYESİ ÖNDER ŞUVAK

GEBZE

2019

GTÜ Fen Bilimleri Enstitüsü Yönetim Kurulu'nun 26./06./2019 tarih ve 2019./29. sayılı kararıyla oluşturulan jüri tarafından 09./07./2019 tarihinde tez savunma sınavı yapılan Osman Yurdakul'in tez çalışması ...Elektronik Mühendisliği...Anabilim Dalında YÜKSEK LİSANS tezi olarak kabul edilmiştir.

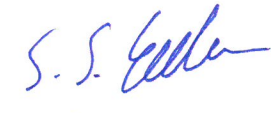
JÜRİ

ÜYE

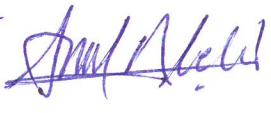
(TEZ DANIŞMANI)

: Dr. Öğretim Üyesi Önder SIVAK 

ÜYE

: Doç. Dr. Serdar Süer ERDEM 

ÜYE

: Dr. Öğretim Üyesi Anıl GELEBİ 

ONAY

Gebze Teknik Üniversitesi Fen Bilimleri Enstitüsü Yönetim Kurulu'nun
...../...../..... tarih ve/..... sayılı kararı.

SUMMARY

In this thesis study, a wideband PLL based frequency synthesizer operating at frequencies between 2070 MHz and 4070 MHz with low phase noise is designed and prototyped. Designed frequency synthesizer is used as local oscillator in an S-band receiver system. Single chip with integrated VCO is used to implement fractional-N frequency synthesizer. Simulations are done to determine loop bandwidth. Measurements are fulfilled with components ensuring determined loop bandwidth. PCB routing is realized in accordance with transmission line impedance for RF signals. Configuring and programming synthesizer are done by utilizing SPI interface of a microcontroller unit. In spite there is a few dB difference, phase noise measurement results are obtained to be close to simulation results. Phase noise for implemented board is obtained at 10 kHz as -87 dB/Hz to carrier and at 100 kHz as -105 dB/Hz to carrier.

Keywords: PLL, Voltage-controlled Oscillator, dB, Phase Noise, Fractional-N Synthesizer, PCB.

ÖZET

Bu tez çalışmasında, 2070 MHz ile 4070 MHz frekans bandında çalışan düşük faz gürültülü faz kilitlemeli çevrim tabanlı bir frekans sentezleyici tasarlanıp gerçekleştirilmektedir. Tasarlanan sentezleyici bir S-band almaç cihazında yerel osilatör olarak kullanılmaktadır. Kesirli-bölen frekans sentezleyiciyi gerçeklemek için dahili gerilim kontrollü salıngaç içeren tümleşik yonga kullanılmaktadır. En iyi çevrim band genişliğini belirlemek için benzetimler yapılmaktadır. Ölçümler en iyi band genişliğini veren çevrim filtresini oluşturan elemanlar ile gerçekleştirilmektedir. Baskılı devre kartı, yüksek frekans çizim teknikleri dikkate alınarak tasarlanmaktadır. Kontrol ve programlama seri arayüz aracılığı ile mikrodenetleyici kullanılarak yapılmaktadır. Ölçüm kayıpları, dielektrik malzeme kayıplarının neden olduğu bir kaç dB kötüleşmeye rağmen, faz gürültüsü ölçümleri benzetim sonuçları ile benzerlik göstermektedir. Gerçeklenen sentezleyicinin ölçülen en kötü faz gürültü değerleri, 10 kHz ötede -87 dBc/Hz, 100 kHz ötede -105 dBc/Hz olarak ölçülmektedir.

Anahtar kelimeler: Faz Kilitlemeli Çevrim, Gerilim-kontrollü Salıngaç, dB, Faz Gürültüsü, Kesirli-bölen Sentezleyici, Baskılı Devre Kartı.

ACKNOWLEDGEMENTS

Foremost, I am grateful to my supervisor Dr. Önder ŞUVAK for his leading and precious suggestions.

I am very grateful to my mother Gülcan YURDAKUL and my sister Yeşim YURDAKUL for their support and encouragement for my whole life.

I am also thankful to my best friend Işıl KİREZ who always has supported and motivated me during the thesis period.

Last but not least, I would like to thank my colleague Onur CUMURCU who helped me with obtaining laboratory measurement results.

TABLE of CONTENTS

	<u>Page</u>
SUMMARY	v
ÖZET	vi
ACKNOWLEDGEMENTS	vii
TABLE of CONTENTS	viii
LIST of ABBREVIATIONS and ACRONYMS	x
LIST of FIGURES	xi
LIST of TABLES	xiii
1. INTRODUCTION	1
2. THEORY of PLL-BASED RF SYNTHESIZERS	3
2.1. Basics of PLL-based RF Synthesizer	3
2.2. Building Blocks of PLL-Based Frequency Synthesizer	5
2.2.1. Phase and Frequency Detector	5
2.2.2. Loop Filter	12
2.2.3. Voltage-Controlled Oscillator	12
2.2.4. Frequency Divider	14
3. PLL-BASED SYNTHESIZER ARCHITECTURES	18
3.1. Integer-N RF Synthesizer	18
3.2. Fractional-N RF Synthesizer	20
3.2.1. Sigma – Delta (Σ - Δ) Fractional-N Synthesizer	23
3.3. Spurs in PLL Based Frequency Synthesizer	24
3.3.1. Reference Related Spurs	25
3.3.2. Integer Boundary Spurs	26
3.3.3. Fractional Spurs	27
3.4. Phase Noise Phenomenon in Frequency Synthesizers	28
3.4.1. Determining Optimum Loop Bandwidth For A PLL Frequency Synthesizer	31
3.4.2 Phase Noise Prediction For A PLL Frequency Synthesizer	32
3.4.3 Phase Noise Improvement in PLL Frequency Synthesizers	32
4. DESIGN OF PLL-BASED RF SYNTHESIZER	34

4.1. Frequency Synthesizer IC Overview	34
4.1.1. Reference Input Circuitry	35
4.1.2. Phase-Frequency Detector and Charge Pump Circuitry	36
4.1.3. Loop Filter Circuitry	36
4.1.4. VCO and Output Stage Circuitry	37
4.1.5. RF Feedback Divider Circuitry	38
4.2. Simulation of PLL Frequency Synthesizer	40
4.2.1. Determination of Loop Bandwidth	42
4.2.2. Characteristics of PLL Frequency Synthesizer	44
4.2.3. Phase Noise Simulation	47
4.3. Design and Implementation	48
4.3.1. Board Material	49
4.3.2. Design Method For PLL Circuits	49
4.3.3. Design Method For Power Supply Circuits	50
4.3.4. Design Method For Digital Circuits	51
4.3.5. Implementing Frequency Synthesizer	52
4.3.6. Configuring Operation Parameters	54
4.3.7 Measurements	55
5. CONCLUSION AND FUTURE WORKS	61
REFERENCES	63
BIOGRAPHY	65
APPENDICES	66
Appendix A: Publications within the Scope of Thesis	66

LIST of ABBREVIATIONS and ACRONYMS

<u>Abbreviations and Acronyms</u>	<u>Explanations</u>
Σ - Δ	: Delta-Sigma
BW	: Bandwidth
CMOS	: Complementary Metal Oxide Silicon
COMINT	: Communication Intellegience
CP	: Charge Pump
dB	: Decibel
dBm	: Decibel to 1 mW
dBc	: Decibel to Carrier
DC	: Direct Current
Hz	: Hertz
LF	: Loop Filter
LFCSP	: Lead Frame Chip Scale Package
LO	: Local Oscillator
OCXO	: Oven-controlled Crystal Oscillator
PCB	: Printed Circuit Board
PFD	: Phase-frequency Detector
PLL	: Phase Locked Loop
ppb	: Pulse per Billion
RF	: Radio Frequency
SPI	: Serial Peripheral Interface
XOR	: Exclusive OR
VCO	: Voltage-controlled Oscillator

LIST of FIGURES

<u>Figure No:</u>	<u>Page</u>
2.1: Concept of an RF synthesizer.	3
2.2: Simple block diagram for PLL RF synthesizer.	4
2.3: A mixer.	7
2.4: A simple XOR gate and its input/output signals.	8
2.5: Plot of the V_{PD} vs. $\Delta\Phi$.	9
2.6: A phase-frequency detector (a) circuit. (b) state diagram.	10
2.7: A reset delayed PFD integrated with charge pump.	10
2.8: Transfer characteristics of phase - frequency detector.	11
2.9: (a) A passive loop filter. (b) an active loop filter.	12
2.10: Transfer characteristics of a VCO.	13
2.11: A simple transistor level VCO circuit.	13
2.12: Single Modulus Prescaler in PLL system.	14
2.13: Dual Modulus Prescaler in PLL system.	15
2.14: Quadruple Modulus Prescaler in PLL system.	16
3.1: Dual-modulus prescaler diagram.	19
3.2: Concept of the fractional division.	21
3.3: Dual-modulus divider controlled by an accumulator.	22
3.5: Adjacent channel interference due to reference related spur.	24
3.6: Current spikes caused by CP mismatch.	25
3.7: Reference related spurs at multiples of 1MHz PFD frequency.	26
3.8: Example of fractional-N loop.	27
3.9: Linear phase noise model of a PLL based synthesizer.	28
3.10: (a) optimum loop BW (b) after intersection (c) before intersection.	31
3.11: Phase noise illustration.	32
3.12: Phase noise contributors and their effective regions.	33
4.1: Conceptual diagram of S-band COMINT receiver.	34
4.2: Functional block diagram of ADF5355 synthesizer IC.	35
4.3: Functional block diagram of ADF5355 PFD/CP circuitry .	36
4.4: Open loop phase noise of ADF5355 internal VCO at 3.4GHz.	37
4.5: ADF5355 output stage.	38
4.6: N Divider functional block diagram.	39

4.7:	Simulated phase noise for OCXO.	41
4.8:	Phase noise of VCO at 4.07 GHz.	41
4.9:	Phase noise at different loop BWs.	42
4.10:	Purposed 3rd order loop filter circuitry.	44
4.11:	Simulated schematics of ADF5355 synthesizer.	45
4.12:	(a) open loop gain (b) closed loop gain of proposed PLL system.	46
4.13:	(a) frequency error (b) phase error while (c) frequency characteristics.	47
4.15:	Simulated phase noise response at 2070 MHz.	48
4.16:	KiCad along with project navigator and toolbars	49
4.17:	AppCAD tool 50 Ω RF line calculation.	50
4.18:	+5 V regulator circuitry.	51
4.19:	SPI signal level translation.	52
4.20:	ATmega328P based Arduino Nano board.	52
4.21:	RF subsystem schematics.	53
4.22:	Power subsystem schematics.	53
4.23:	PCB drawing	55
4.24:	3D illustration of frequency synthesizer.	56
4.25:	Power supply current drawn by the board.	56
4.26:	Output spectrum	57
4.27:	Harmonic response measurement.	57
4.28:	4.07 GHz phase noise result at (a) 10 kHz and (b) 100 kHz.	58
4.29:	2.07 GHz phase noise result at (a) 10 kHz and (b) 100 kHz.	59

LIST of TABLES

<u>Table No:</u>	<u>Page</u>
4.1: Specifications for 10 MHz OCXO.	40
4.2: Frequency switching time at various loop BW.	43
4.3: Frequency switching time at different phase margin.	43
4.4: Loop BW and phase margin for calculated and used filter components.	44
4.5: Phase noise result for 2070 MHz and 4070 MHz.	60
4.6: Specification of the synthesizer.	60

1. INTRODUCTION

A frequency synthesizer is an important part of radio frequency (RF) communication system. It generates oscillations at different range of frequencies and takes place as local oscillator (LO) in transmitters and receivers. Frequency synthesizers may carry out multiplication, division and mixing operations to generate desired radio frequency.

Frequency synthesis techniques can be classified in two main groups such as direct and indirect frequency synthesis. Direct synthesis is consist of direct digital synthesis (DDS) and direct analog synthesis (DDS). Indirect synthesis is realized by phase-locked loop (PLL) technique [1]. The most common type of the frequency synthesizers that used in RF applications is the PLL-based frequency synthesizers (FS) because of their adequate performance, ease of integration and moderate power dissipation.

The PLL-based RF synthesizers which are used in radio receivers should have some key performance criteria such as spectral purity (harmonics, phase noise, spurs) and timing (frequency switching speed). Spectral purity is an important issue when FS is used as LO in a receiver. SNR is a function of phase noise level of the LO [2], [3]. SNR ratio is important parameter which determines the sensitivity of a receiver. Bad spectral density disturbs the receiving weak signals [4]. Therefore, spectral purity is an important performance criteria for a receiver applications. Switching speed determines how fast frequency synthesizer switches from one frequency to another. It can be defined as time spent by synthesizer during this switching between two states. Sweeping time is an important criteria in RF signal reception. When a receiver sweeps a particular frequency band, frequency switching speed of LO of that receiver is an important criteria to define sweep speed of the receiver.

This thesis includes designing, simulating and implementing of a phase-locked loop based RF synthesizer is achieved.

The thesis is composed of five chapters. Chapter 2 presents detailed discussion of phase-locked loop based RF synthesizer.

This chapter begins with the basics of PLL, working principle and blocks that build phase-locked system loop are explained.

Chapter 3 mentions different types of PLL-based RF synthesizers such as integer-N and fractional-N frequency synthesizer. The chapter is completed with spurious types in PLL, phase noise phenomenon subjects.

Chapter 4 is dedicated for designing, simulating and implementing of PLL-based frequency synthesizer which is utilized as local oscillator in a COMINT (Communication Intelligence) receiver which cover the band from 2 GHz to 4 GHz . While computer based design is done by Altium software, simulation is done by ADISimPLL software which is a trademark of Applied Radio Labs. Discrete commercial components are used in the design of frequency synthesizer. Specifications of the components are specified in the simulation software and component values of the loop filter are adjusted for optimum phase noise performance and locking time performance. After that system is realized on the printed circuit board (PCB) with commercial components. In this chapter simulation results and measurement from the PCB is presented.

Chapter 5 which is conclusion chapter is dedicated to summary of this study, explanation of important points and things are possible to be done in the future.

2. THEORY of PLL-BASED RF SYNTHESIZERS

In this chapter, the fundamentals of PLL-based frequency synthesizers are explained. First, general overview of PLL-based frequency synthesizers is given. Then, building blocks of PLL-based frequency synthesizer is discussed in detail.

2.1. Basics of PLL-based RF Synthesizer

An equipment producing a set of output frequencies by using reference input signal can be defined as an RF synthesizer. It is illustrated in Figure 2.1 [1].

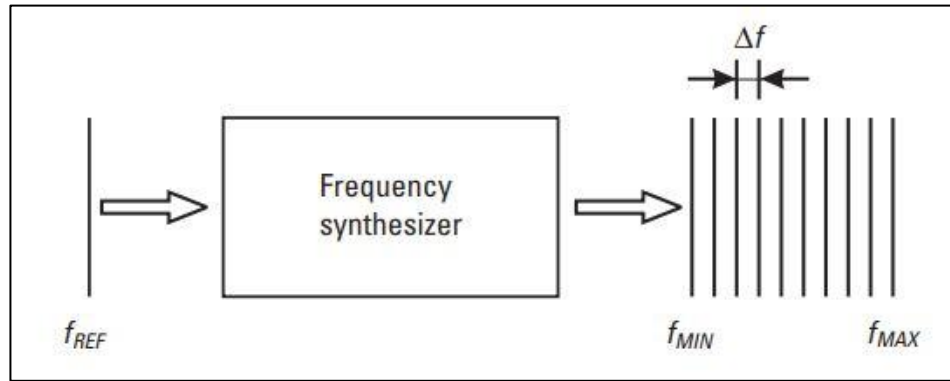


Figure 2.1: Concept of an RF synthesizer.

PLL-based RF synthesizer uses phase-locked loop technique to produce output frequencies from stable and precision reference source. PLL is a closed loop feedback system that compares signal sampled from output and reference signal both in frequency and in phase [1]. Figure 2.2 [1] shows a basic diagram.

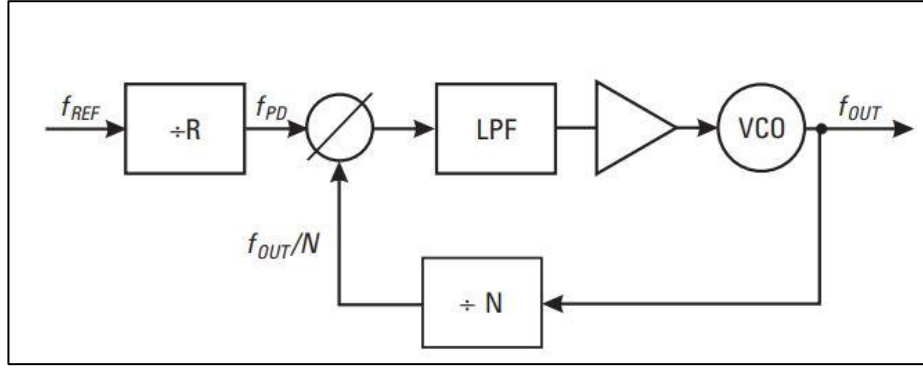


Figure 2.2: Simple block diagram for PLL RF synthesizer.

Operation of the PLL system is dependent on technology. Fundamentally, R prescaler divides the frequency of the reference signal and N feedback divider divides the frequency of the output signal. The frequency-divided signals are compared in frequency and phase by phase-frequency detector (PFD). PFD generates an error signal that is in proportional to phase and frequency difference between the compared signals. Error signal generated by PFD is converted into DC value by loop filter (LF) which is a low-pass filter that eliminates high frequency components on the error signal. DC value is used to tune voltage-controlled oscillator (VCO). VCO is an oscillator that generates frequency according to the tune voltage which is applied to the input of the VCO. If DC value is not enough for VCO to produce the desired frequency, an operational amplifier should be placed between LF and VCO. This means an active filter should be used. But, active filter adds extra noise, complexity and cost to the system. When phase difference is zero or constant and there is no frequency difference between the compared signals, the system is locked and stabilized. If a different output frequency is intended to be generated, the N divider which divides output frequency is programmed accordingly. As long as the PLL is in lock state, the output frequency is expressed as in (2.1) [1].

$$F_{OUT} = \frac{N}{R} \times F_{REF} \quad (2.1)$$

If N divider value is an integer, then PLL is called integer-N PLL. Frequency resolution (channel spacing) of an integer-N PLL is equal to the frequency of the PFD that is F_{REF} / R . Provided that the PLL is fractional-N, N is a fractional value. In this situation, frequency resolution can be less than the frequency of the PFD. To

improve phase noise performance of the frequency synthesizer, N counter value should be selected as low as possible [1].

2.2. Building Blocks of PLL-Based Frequency Synthesizer

A PLL-based frequency synthesizer consists of the following parts,

- A phase or phase-frequency detector (PFD), which compares input reference signal (REF) and divided VCO output signal in phase and frequency and generates an error signal depending on phase and frequency difference.
- A charge pump (CP), which sources or sinks current in accordance with the signal coming from PFD.
- A loop filter (LF), which filters high frequency contents of error signal from PFD out and convert it into a DC level. LF realizes a low-pass filtering operation.
- A voltage-controlled oscillator (VCO), which produce an oscillation proportionally to the DC tuning voltage coming from LF.
- A frequency divider, which divides the VCO frequency to create a frequency which is equal to input reference frequency.

2.2.1. Phase and Frequency Detector

While a phase and frequency detector (PFD) is a circuitry that compares phase and frequency difference between reference source and VCO frequency-divided output and generates an error function proportional to difference [15], [16], [23]. A phase detector performs same thing comparing only phase of the input signals. The gain of the phase or phase-frequency detector ($K_{PFD/PD}$) is given by,

$$K_{PFD/PD} = V_D \times \Delta\Phi \quad (2.2)$$

where V_D is the average voltage value of the error signal, and $\Delta\Phi$ is the phase difference between inputs applied to phase detector. While phase detectors can be

examined as exclusive-OR based PD and mixer based PD, PFD is examined as tri-state phase - frequency detector.

2.2.1.1. Multiplier (Mixer) Based Phase Detector

A mixer can be utilized as phase detector and it is illustrated in Figure 2.3. A mixer has two input and one output and gives both the sum and difference frequencies at the output [1], [17]. Input signals are sinusoidal such as $V_1 = A_1 \sin(\omega_1 t + \theta_1)$ and $V_2 = A_2 \sin(\omega_2 t + \theta_2)$ and the output is described by,

$$V_{OUT} = A_1 \sin(\omega_1 t + \theta_1) \times A_2 \sin(\omega_2 t + \theta_2) [V] \quad (2.3)$$

after utilizing trigonometric transformations, the output is expressed by,

$$V_{OUT} = \frac{A_1 A_2}{2} \cos[(\omega_1 - \omega_2)t + (\theta_1 - \theta_2)] - \frac{A_1 A_2}{2} \cos[(\omega_1 + \omega_2)t + (\theta_1 + \theta_2)] [V] \quad (2.4)$$

and placing a low pass filter at the mixer output that eliminates high frequency content which is sum product of the inputs, the output signal reduces to,

$$V_{OUT} = \frac{A_1 A_2}{2} \cos[(\omega_1 - \omega_2)t + (\theta_1 - \theta_2)] [Volts] \quad (2.5)$$

Mixer phase detectors cannot sense frequency difference but phase difference. Therefore, the frequencies of input signals are the same and frequency content $(\omega_1 - \omega_2)t$ of the output is equal to zero. Thus, the output of the mixer PD provides DC signal in proportional to phase difference $(\theta_1 - \theta_2)$. The mixer used as phase detector needs to be a balanced mixer, otherwise an unwanted DC voltage offset is presented at the output [1]. The other unwanted signals at the output spectrum are input reference signal and sum of frequency of reference signal and divided frequency of VCO signal. These unwanted frequencies are eliminated by low pass filter.

Its contribution to overall phase noise is low and its capability to support high frequency reference input are the main advantages of this type of PD. On the other hand, unwanted DC offset arising from its imperfect balance, unwanted frequency products (harmonics, etc.) and not having frequency discrimination are among its disadvantages [1].

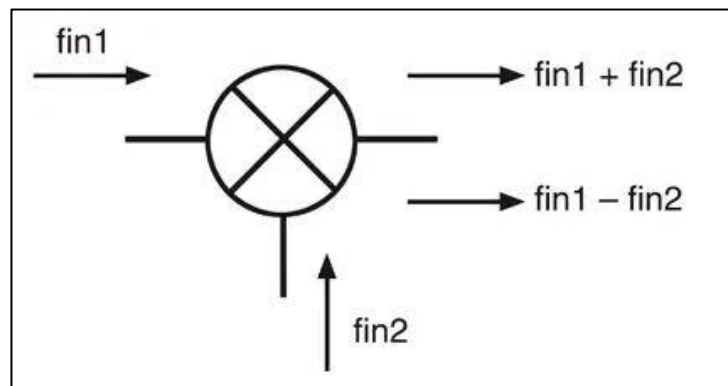


Figure 2.3: A mixer.

2.2.1.2. XOR Based Phase Detector

That is implemented by using XOR logic gate. The inputs are in square form. When input signals have no phase difference in , the output of the PD is at zero volt. When the phase difference between the input signals is 180° , the output is high depending on the supply voltage of the XOR gate. Between 0° and 180° , the gate outputs a pulse train. Using a simple low-pass filtering at the output of the gate, an average voltage is obtained which is proportional to the phase difference and the supply voltage of XOR gate (VDD). Frequency of the PD output signal is equal to twice the input reference signal [1]. Simple XOR gate and its input and output signals are shown in Figure 2.4 [1].

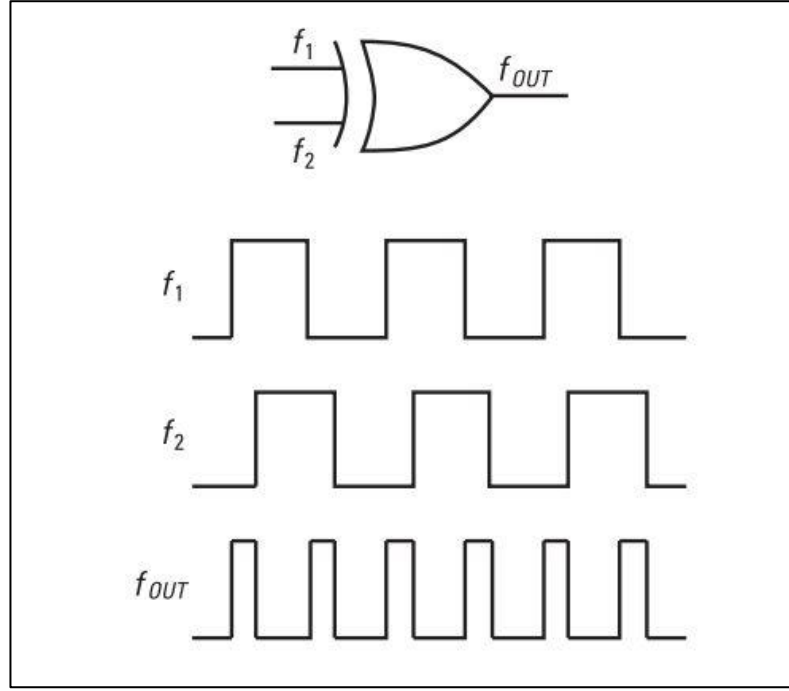


Figure 2.4: A simple XOR gate and its input/output signals.

The XOR-based PD operates similarly as mixer based PD. XOR-based PD does also not have a frequency discriminator. Therefore, The input signals need to be 50% duty cycle and same frequency for proper operation [1].

The phase difference between input reference signal and divided VCO signal expressed as,

$$\Delta\Phi = \Phi_1 - \Phi_2 = \frac{\Delta t}{T_2} \times 2\pi = \frac{\Delta t}{T_{out}} \times \pi \text{ [radians]} \quad (2.6)$$

Average output voltage is given by,

$$V_{PD} = \frac{\Delta\Phi}{\pi} \times V_{DD} = K_{PD} \times \Delta\Phi \text{ [Volts]} \quad (2.7)$$

K_{PD} is the gain of the phase detector. The plot of average voltage versus phase difference is illustrated in Figure 2.5 [18].

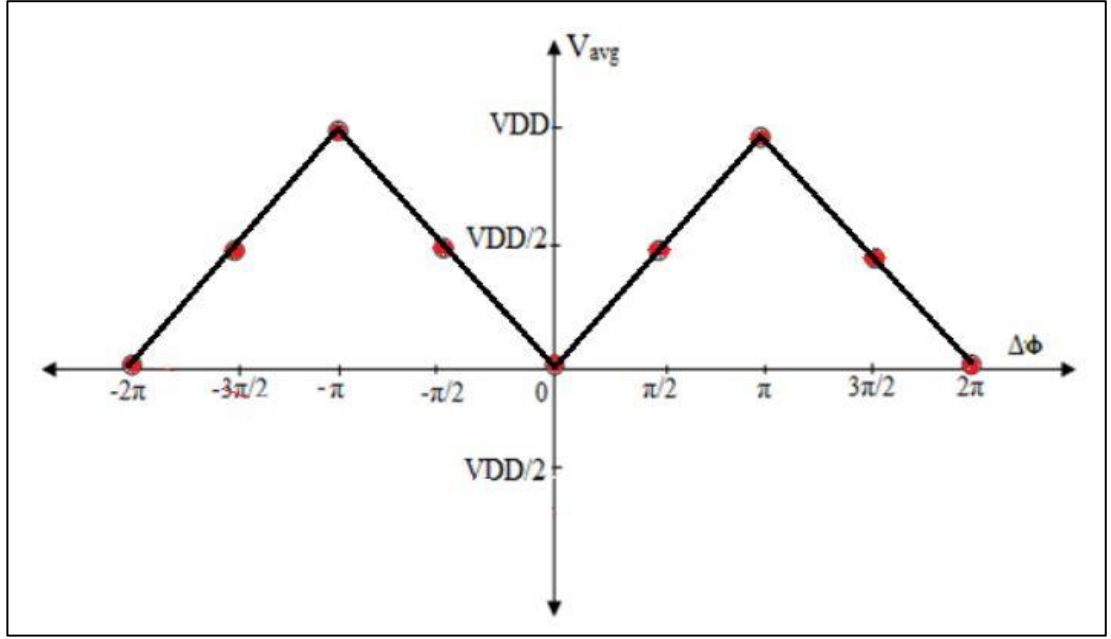


Figure 2.5: Plot of the V_{PD} vs. $\Delta\Phi$.

2.2.1.3. Tri-state Phase - Frequency Detector

Mixer and XOR-based phase detectors are not able to detect frequency difference between reference signal and divided VCO signal and are not appropriate for the PLL-based frequency synthesizers where the divided VCO frequency is different from reference signal frequency. PFD is generally implemented as a circuit consisting of D flip-flop combined with charge pump structure as illustrated in Figure 2.6a [1]. The PFD has two output called up and down. When up output is high, the frequency of VCO is incremented. A high signal at down output causes the VCO to decrease its output frequency [1] [15].

Upper flip-flop controls PMOS transistor of the charge pump while lower flip-flop controls NMOS transistor [8].

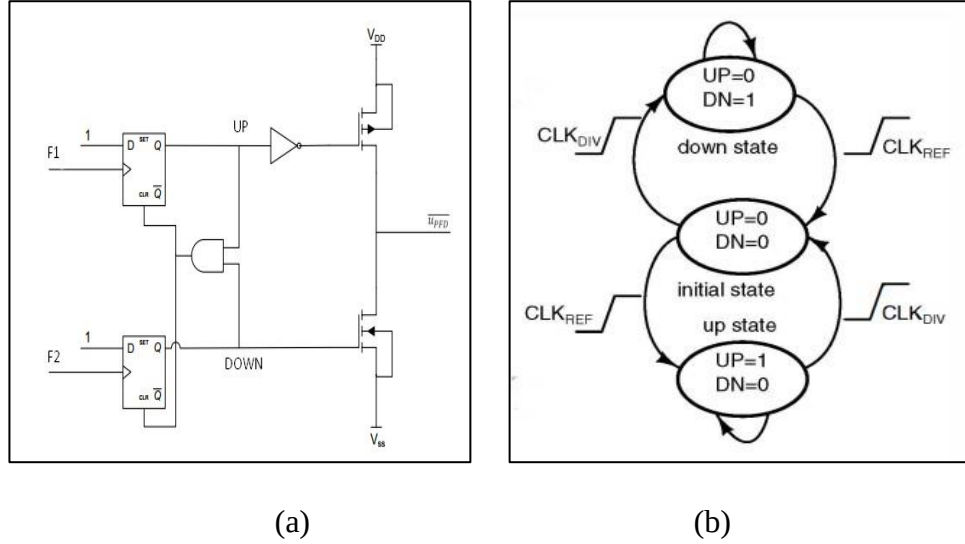


Figure 2.6: A phase-frequency detector (a) circuit. (b) state diagram.

The state diagram of tri-state PFD is shown below in Figure 2.6b [20]. The PFD is not able to sense a too small differences in phase between reference signal and divided VCO output. Hence no current sinking or sourcing occurs in the charge pump. This creates a phenomenon called dead zone. Dead zone is able to be eliminated by placing a delay element onto reset path of D flip-flops as shown in Figure 2.7 [7].

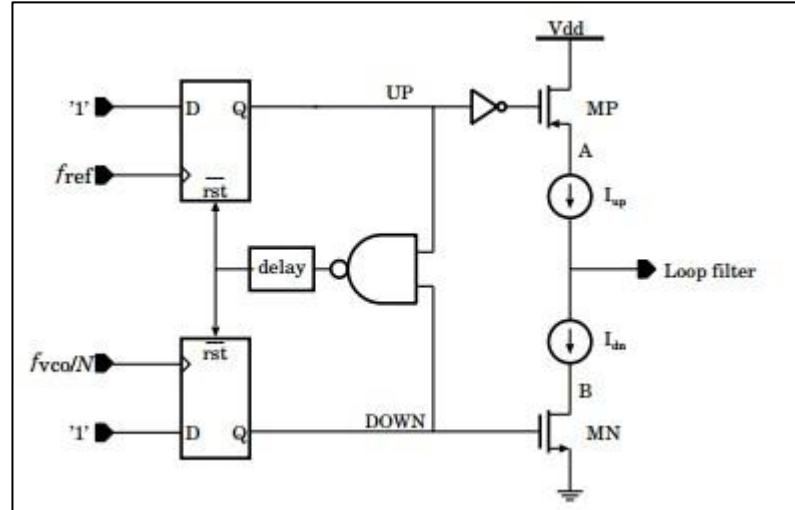


Figure 2.7: A reset delayed PFD integrated with charge pump.

CLK_{REF} or F1 is the frequency of reference signal and CLK_{DIV} or F2 is the frequency of divided VCO signal which is coming from frequency divider placed onto feedback line within the PLL loop. When CLK_{REF} leads CLK_{DIV}, CLK_{REF}

triggers the upper flip-flop and UP which is output of the upper flip - flop is switched from low (0) to high (1) which starts current sourcing and DOWN which is output of the lower flip-flop keeps its state which is low. As sourcing current provided that a rising edge of CLK_{DIV} signal, both flip-flops are reset, both transistors are switched off and the output becomes high impedance (high-Z). Similar events happen when CLK_{REF} lags CLK_{DIV} but, this time, NMOS transistor is ON and current is sinking instead of sourcing [8].

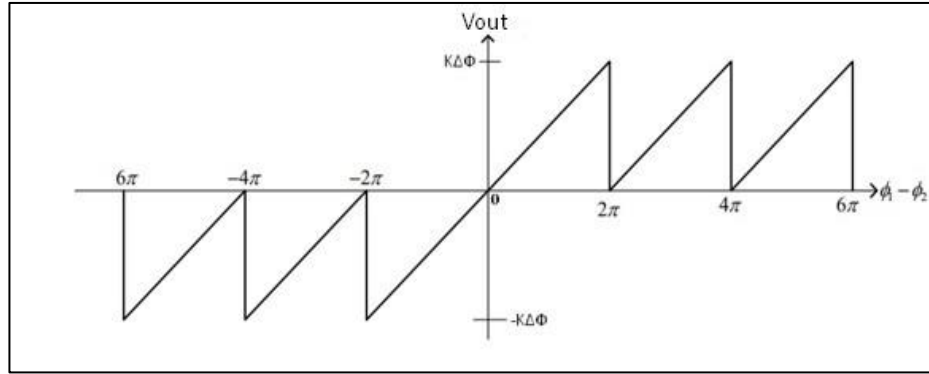


Figure 2.8: Transfer characteristics of phase - frequency detector.

Transfer characteristics of a phase – frequency detector is illustrated in figure 2.8 [15]. PFD has three different modes of operation. If $\Delta\Phi$ is larger than $\pm 2\pi$, PFD is in frequency detection mode where the PFD continually sources or sinks depending on which signal's frequency is higher. When $\Delta\Phi$ is smaller than $\pm 2\pi$ PFD is in phase detection mode in which the charge pump is active only during a portion of the period which is defined by the phase difference. In phase-frequency locked mode, the phase difference is zero and the output is at high-Z [21].

The average output voltage of the PFD proportionally changes with phase difference, if PFD is in phase detection mode. PFD characteristics is periodical with 2π . Average output voltage is given by

$$V_{PFD} = K_{PFD} \times \Delta\Phi \text{ [Volts]} \quad (2.8)$$

2.2.2. Loop Filter

Phase detector output signal includes a DC component and high frequency contents. Voltage controlled oscillator requires DC tuning voltage at its input to produce a frequency content. Therefore a loop filter which implies a low pass filtering to PFD output signal is used to get DC tuning voltage. Loop filter can be in active or passive topologies. When charge pump supply is below VCO tuning voltage range, the average output voltage needs to be scaled to this tuning range. In this case, an active filter topology is used to scale. Otherwise, a passive loop filter topology can be used. A passive and an active loop filter is shown in figure 2.9a and figure 2.9b [8], respectively.

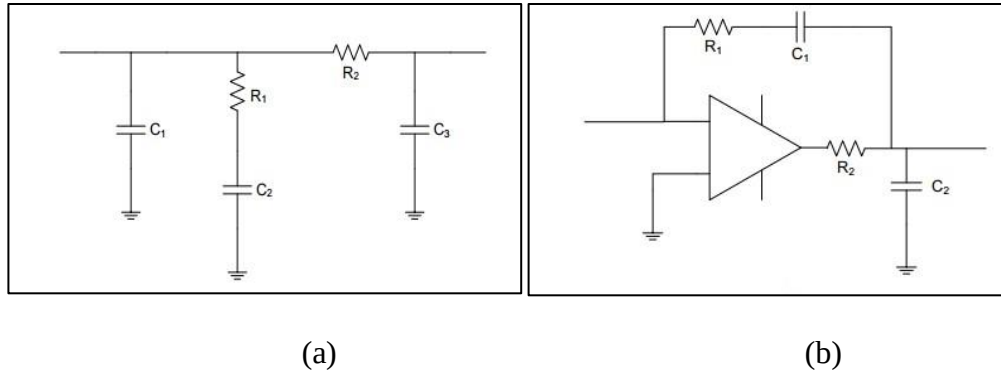


Figure 2.9: (a) A passive loop filter. (b) an active loop filter.

2.2.3. Voltage-Controlled Oscillator

Voltage-controlled oscillator is the key component in PLL synthesizers that generates the purposed frequency output [9]. Conceptional block diagram and desired behavior of VCO is shown in figure 2.10 [4]. The output frequency changes from ω_1 to ω_2 while the control voltage (V_{CONT}) varies from V_1 to V_2 . The slope of this characteristics, K_{VCO} is stated as sensitivity or gain of the VCO and expressed in rad.Hz/V. It is given by,

$$\omega_{OUT} = K_{VCO} \times V_{CONT} + \omega_0 \text{ [rad. Hz]} \quad (2.9)$$

where ω_0 states intercept point on the frequency axis. K_{VCO} is desired not to change

significantly within tuning range [4].

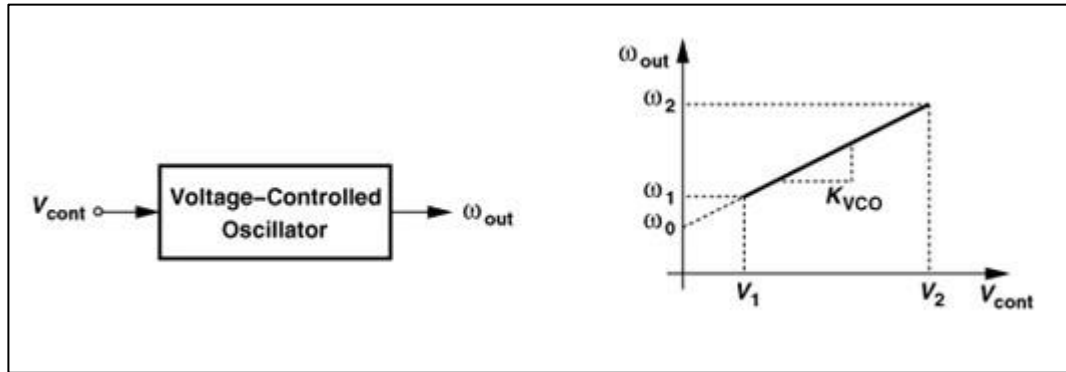


Figure 2.10: Transfer characteristics of a VCO.

In spite there exists different types of oscillators, in RF applications, oscillators that are resonator based are commonly used. A typical VCO is illustrated in figure 2.11 [8]. Output frequency is varied by changing voltage on the varactor (voltage-controlled capacitor) which adjust resonance frequency. Active device provides negative resistance to compensate resonator loss and supplies stable oscillation [8].

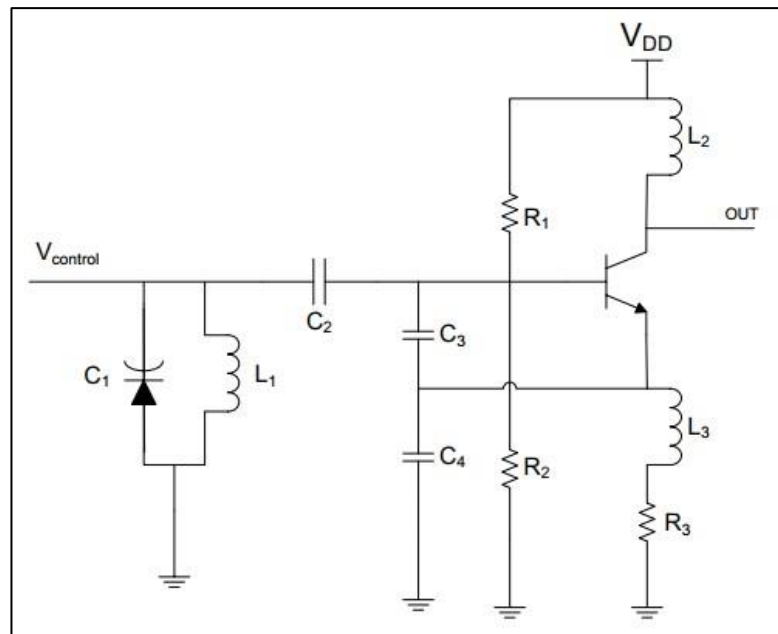


Figure 2.11: A simple transistor level VCO circuit.

2.2.4. Frequency Divider

Frequency divider is a device that divides the frequency of input signal by N which is the division ratio [1]. Frequency dividers are used on feedback line in PLL systems. Their objective is to divide VCO output frequency in order to be able to compared input reference frequency by phase-frequency detector. For low frequencies less than 200 MHz, counters can be used as frequency divider. However, digital counters are unable to handle high frequency (high VCO frequencies in PLL system). Therefore prescalers which have ability in handling high frequency input signals are used in front of digital counter to decrease the frequency to the levels that counter is able to handle [12]. Dividers can be classified in accordance with prescaler modulus. These are single modulus, dual modulus and quadruple modulus prescalers.

2.2.4.1. Single Modulus Prescaler

In this approach, single prescaler is combined with a digital counter to create a high frequency frequency divider. Counter is adjusted to B while prescaler is fixed and its value is P . Then division ratio is $N = B.P$. As it can be seen from formula, only integer multiple of P can be generated as N . This is one disadvantage of this type [12]. PLL blocks integrated with single modulus is illustrated in Figure 2.12 [12].

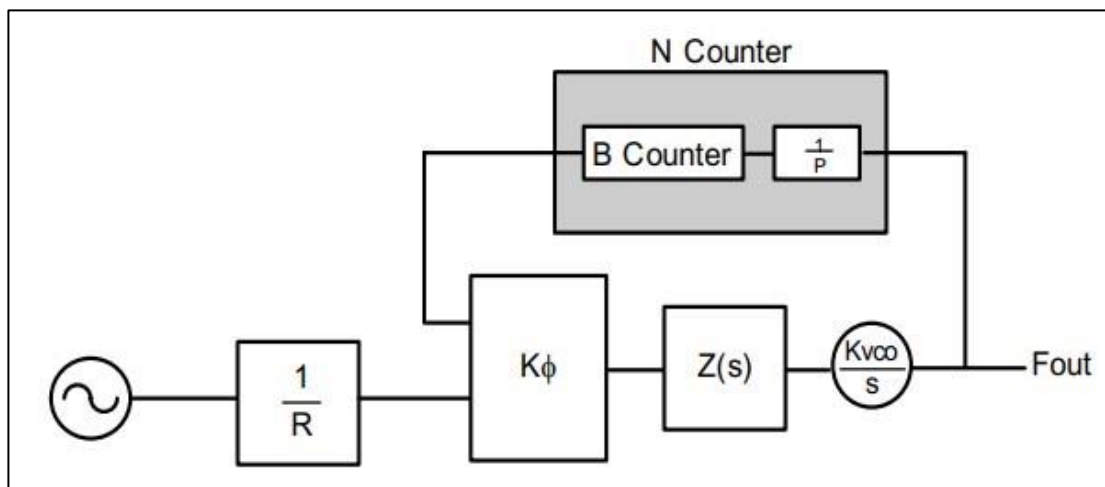


Figure 2.12: Single Modulus Prescaler in PLL system.

2.2.4.2. Dual Modulus Prescaler

In order to get better division resolution, dual modulus is utilized which is shown in Figure 2.13 [12]. This allows its division coefficient to be two different values: P or $P + 1$. In fact, there exists only one prescaler whose value is P , and $P + 1$ coefficient is obtained by implementing a pulse swallow function before the prescaler. In addition to digital counter B in single modulus type, another counter called swallow counter is used to control if pulse swallow function is enabled or not [12].

Throughout A cycles, $P + 1$ prescaler is active, then remaining $B - A$ cycles, P prescaler operates. When B counter finishes counting, reset event occurs and same procedure is repeated. At the end, it gives a division ratio stated in (2.10) which illustrates having better division ratio than single modulus.

$$N = A \cdot (P + 1) + (B - A) \cdot P = B \cdot P + A \quad (2.10)$$

B should be higher than or equal to A is required for proper operation of the prescaler. When this restriction is not satisfied, the B counter finishes counting before A counter and reset event untimely occurs [12]. For instance, in a 32/33 ($P/P+1$) dual modulus prescaler, maximum value for A is 31 ($P-1$) and minimum value for B is 31 which gives a minimum division ratio of 992.

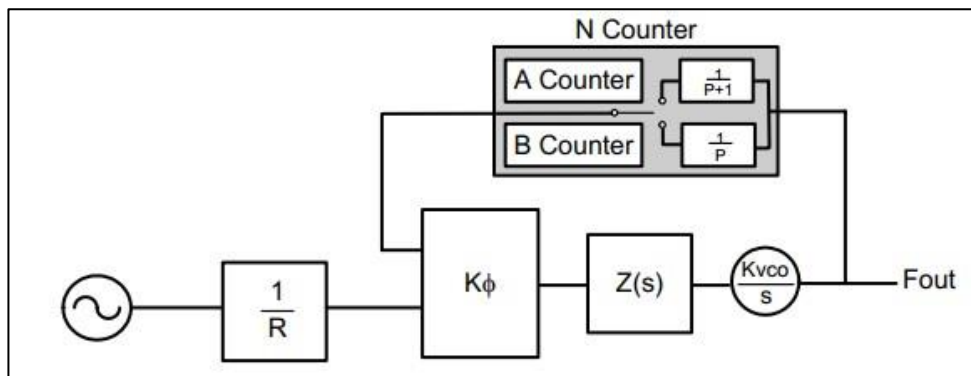


Figure 2.13: Dual Modulus Prescaler in PLL system.

2.2.4.3 Quadruple Modulus Prescaler

So as to get lower minimum division ratio, the quadruple modulus prescaler is used. In quadruple modulus prescaler, there are four prescalers, however depending on the value of A and B, only three of them are utilized to generate any frequency division ratio (N). Operation is very similar to that of dual modulus. All counters begin to count at the same time. For A cycles, P+5 prescaler is enabled. If $B \geq A$, P+4 is enabled for B-A cycles or P+1 is enabled for A-B cycles, if $B < A$. P is active for C-B cycles [12]. At the end when all counters finish counting, it gives N as shown in (2.11).

$$N = A \cdot (P + 5) + (B - A) \cdot (P + 4) + (C - B) \cdot P = C \cdot P + 4B + A \quad (2.11)$$

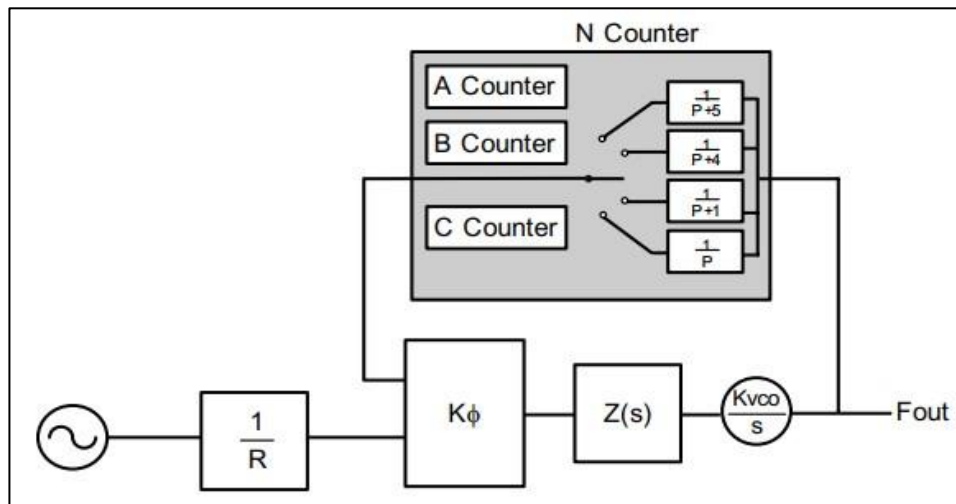


Figure 2.14: Quadruple Modulus Prescaler in PLL system.

There is no restriction on A or B. However, for proper operation, C ought to be greater than maximum of A and B. In comparison to dual modulus prescaler, quadruple modulus prescaler has lower minimum division ratio and increased maximum division ratio. Minimum division ratio is calculated by,

$$N_{MIN} = \max\left\{\left(\frac{P}{4} - 1\right), 3\right\} \times P \quad (2.12)$$

For example, 32/33/36/37 quadruple prescaler, minimum division ratio is calculated, according to (2.12), as 224.

3.PLL BASED SYNTHESIZER ARCHITECTURES

There are two PLL architectures which are integer-N and fractional-N PLL. Provided that N counter value is integer, the PLL is integer-N. It is called fractional-N, when N counter value is fractional [5]. This section provides detailed explanation for these architectures. After these explanations, PLL spurs with reduction techniques are given and the chapter is completed with phase noise of PLL and its importance.

3.1. Integer-N RF Synthesizer

The integer-N architecture is able to synthesize frequency with channel spacing as the PFD frequency or integer multiples of PFD frequency. Let us assume that PFD frequency is 10 MHz. The possible channel spacings are 10 MHz, 20 MHz, 30 MHz, etc. [7]. The N counter determine the division ratio between reference input and output frequencies [8]. This type of divider is commonly implemented with CMOS technology and not good at operating at very high frequency. To extend the operating frequency of the divider, a high-frequency prescaler (P) whose value is constant, is added before the N-divider. However, this method increases the channel spacing of the synthesizer. For instance, if a prescaler is added, the output frequency is determined by:

$$F_{OUT} = (P \times N) \times F_{PFD} \quad (3.1)$$

As seen from (2.2), the step size (channel spacing) becomes $P \times F_{PFD}$. To decrease the channel spacing, F_{PFD} can be decreased. However, this results in deteriorating in locking time and phase noise performance [1].

This restriction is handled by utilizing dual-modulus prescaler topology as illustrated in figure 3.1. The division coefficient of the dual-modulus prescaler is able to be adjusted as P or (P+1). It operates in collaboration with two low-frequency programmable dividers which are marked as A-counter and B-counter. These are clocked by the same prescaler output [1].

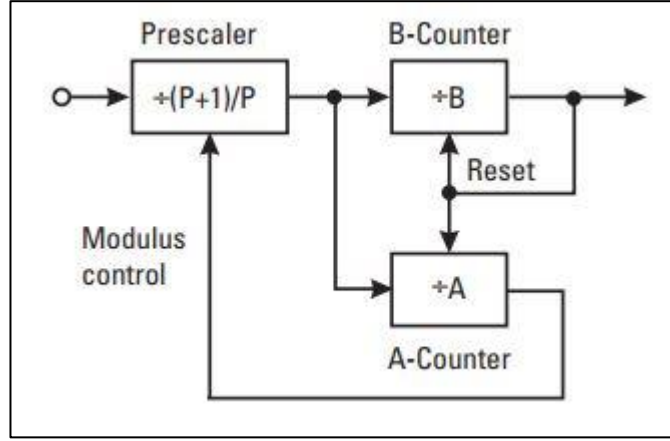


Figure 3.1: Dual-modulus prescaler diagram.

At first, the prescaler divides by $(P + 1)$, up to A counter counts A pulses and changes its division ratio to P. At this moment, the number of pulses is $(P+1)A$. After that, B starts counting and counts $(B-A)$ more pulses with division ratio of P. Now, number of pulses is $P(B-A)$. After a cycle is completed, the division ratio N is;

$$N = (P + 1) \times A + P \times (B - A) = P \times B + A \quad (3.2)$$

Now the output frequency is;

$$F_{OUT} = (P \times B + A) \times F_{PFD} \quad (3.3)$$

The output frequency is able to be tuned in steps F_{PFD} . Thus, the operating frequency of the feedback N-divider is extended without increasing the channel spacing [1].

A and B are integer values which are be able to adjustable. If B is less than A, B-counter resets the system before A-counter changes the prescaler division value. This means, prescaler division ratio is always kept at $(P+1)$. Therefore, B value needs to be more than A value. The minimum division factor is defined by,

$$N = P (P - 1) \quad (3.4)$$

In high frequency operation, P should be high enough so that the other two counters can operate properly. Because, A and B counters operates properly at low frequencies [1].

3.2. Fractional-N RF Synthesizer

As has been explained before, the step size of the synthesizer is determined by the frequency of the PFD. For smaller step sizes without changing the output frequency, PFD frequency must be reduced [6]. Decreasing the frequency of the PFD results in higher N-divider ratio which degrades phase noise performance of the synthesizer [8]. This will be discussed in the next chapters.

Output frequency of a fractional-N is possible to be a fractional multiples of the PFD frequency which implies that the channel spacing is smaller than the PFD frequency. Hence, the step size of the synthesizer is able to be decreased without reducing the frequency of the PFD and N-divider value can be significantly small which provides better phase noise performance than integer-N architecture does [10], [13]. In this architecture, N division ratio can be programmed to a fractional value which is expressed as,

$$N = N_{INTEGER} + \frac{N_{FRACTION}}{N_{MODULUS}} \quad (3.5)$$

The output frequency of the fractional-N frequency synthesizer is given by,

$$F_{OUT} = F_{PFD} \times \left(N_{INTEGER} + \frac{N_{FRACTION}}{N_{MODULUS}} \right) \quad (3.6)$$

where F_{OUT} is the output frequency of the voltage-controlled oscillator, $N_{INTEGER}$ (INT) is the integer part of the division ratio, $N_{FRACTION}$ (FRAC) is the channel number and $N_{MODULUS}$ (MOD) is the fractional resolution in respect of the PFD frequency.

The step size of the system is expressed as,

$$F_{STEP} = \frac{F_{PFD}}{N_{MODULUS}} \quad (3.7)$$

For example, in a fractional-N synthesizer, if the frequency output is 2000.02 MHz and the step size is 10 kHz, the PFD frequency is 25 MHz, then INT value is 80, MOD 2500 and FRAC is 2. In integer-N synthesizer, the PFD frequency must be same with the step frequency. In this case, it is 10 kHz and N division ratio is 200002 which is approximately 2500 times larger than that of the fractional-N synthesizer. A small divider value of the fractional-N architecture helps to decrease the output phase noise of the synthesizer [14]. The fractional division factors are realized by switching two divider as illustrated in figure 3.2 [1].

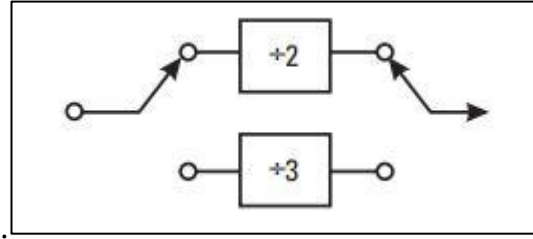


Figure 3.2 Concept of the fractional division.

A part of input pulses are divided by two, and the other part of input pulses are divided by three. The total number of input pulses over the sum of the number of pulses delivered by the divider circuit for a given time interval gives the average division ratio. Simply, let us assume that the input frequency of the divider is 60 MHz (60 million pulses/sec). The half of total pulses (30 million pulses/sec) is divided by two which results in 15 million pulses per second, and by switching the division factor to 3 the other half of the pulses is divided by three which gives 10 million pulses per second. Altogether, the circuit delivers 25 million pulses per second (25 MHz). The average division ratio is 2.4 which is given by $60 \div 25$.

One of the convenient fractional-N synthesizer application utilizes a dual-modulus division concept in its feedback line as demonstrated in Figure 3.3 [1]. An accumulator which is clocked by the feedback divider output is used to manage the division ratio of the feedback divider [1].

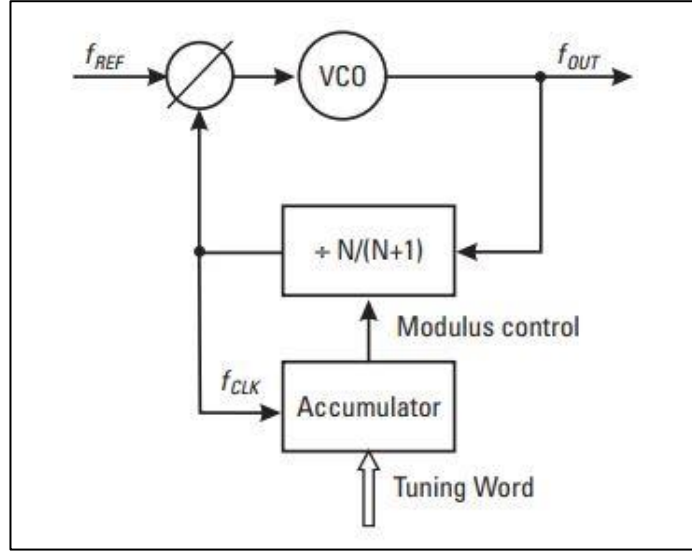


Figure 3.3: Dual-modulus divider controlled by an accumulator.

The preloaded content of the accumulator is incremented on every clock cycle until it reaches its max value and it resets and initializes the process again [1]. $N_{MODULUS}$ is the max value to which the accumulator is able to go up and $N_{FRACTION}$ is the tuning word which is preloaded content of the accumulator. For example, during $N_{FRACTION}$ cycles, division factor is $(N + 1)$ and during the remaining $(N_{MODULUS} - N_{FRACTION})$ cycles, the division factor is N . Then overall division ratio is given by,

$$N_{Overall} = \frac{N_{FRACTION} \times (N + 1) + (N_{MODULUS} - N_{FRACTION}) \times (N)}{N_{MODULUS}} \quad (3.8)$$

which gives the same statement in (2.6). In this concept, a sudden change in division factor between N and $(N + 1)$ gives rise to an instantaneous phase error that generates fractional spurs at frequencies of the step size. Unless, they are eliminated, they can be inconvenient. Although, these spurs are low, they settle down into loop bandwidth. The fractional spurs are the major difficulty of fractional- N synthesizers.

There are different phase correction methods such as current injection, delay line control, DAC compensation which are analog techniques can be easily affected by process, temperature and voltage variations [12]. To minimize fractional spurs using Σ - Δ modulator instead of the accumulator.

3.2.1. Sigma – Delta (Σ - Δ) Fractional-N Synthesizer

As discussed in the previous chapter, the fundamental concept of fractional-N synthesizer is to acquire a fractional division ratio switching between two integer factors. The switching management is realized by an accumulator which is essentially a 1st order Σ - Δ modulator. However, Σ - Δ fractional-N synthesizers refers to have at least 2nd order Σ - Δ modulator in its divider circuit. Nth order Σ - Δ modulator alternates the division factor among 2^N integer values. When the order of the modulator is increased which pushes the fractional spurs to the beyond cut-off frequency of loop filter, low pass filtering reduces the spur levels. [12].

Simple Σ - Δ modulator can be modeled as in Figure 3.4 [12]. Instantaneous phase error is added to ideal divider. The instantaneous phase error is expressed by $E(z)$ and Z^{-1} represents delay for one clock cycle.

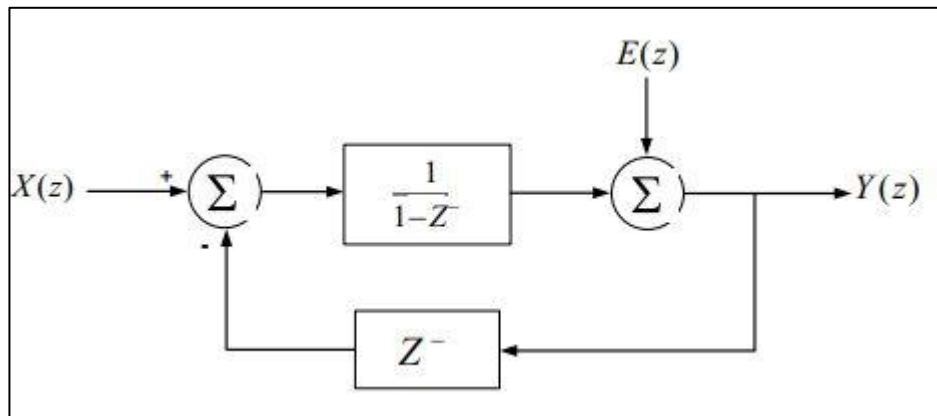


Figure 3.4: 1st order Σ - Δ modulator model.

Output is expressed as,

$$Y(z) = X(z) + E(z)(1 - Z^{-1}) \quad (3.9)$$

As seen from (3.8), Difference between current phase error and previous phase error values ensures a digital high pass filtering process. When Σ - Δ modulator is mentioned, it is second or upper order modulator. Transfer function for nth order Σ - Δ modulator is given by,

$$Y(z) = X(z) + E(z)(1 - Z^{-1})^n \quad (3.10)$$

Higher order Σ - Δ modulators move the phase error to higher frequencies. Thus, the noise can be filtered out more efficiently by loop filter. Beside of increasing modulator order, Σ - Δ fractional-N synthesizers utilizes dithering method to reduce fractional spur levels which are occurs at channel spacing frequency. Dithering is a method of adding randomness to alternating division factors to reduce the periodicity. Thus, the energy of the fractional spurs at low frequencies is moved to higher frequencies which are be able to be eliminated by the loop filter [12].

3.3. Spurs in PLL Based Frequency Synthesizer

Spurs are noise that intensified at a certain offset frequency from carrier frequency. These offset frequencies typically are multiples of the synthesizer channel spacing. Adjacent channel is mixed down by this spurs which gives rise undesired products to fall into desired bandwidth [12] as shown in figure 3.5 [22]. In this regard, spurious response of a frequency synthesizer is an important concern. In respect of the reasons of spurs, there are different types such as reference related spurs, integer boundary spurs (IBS) and fractional spurs [8].

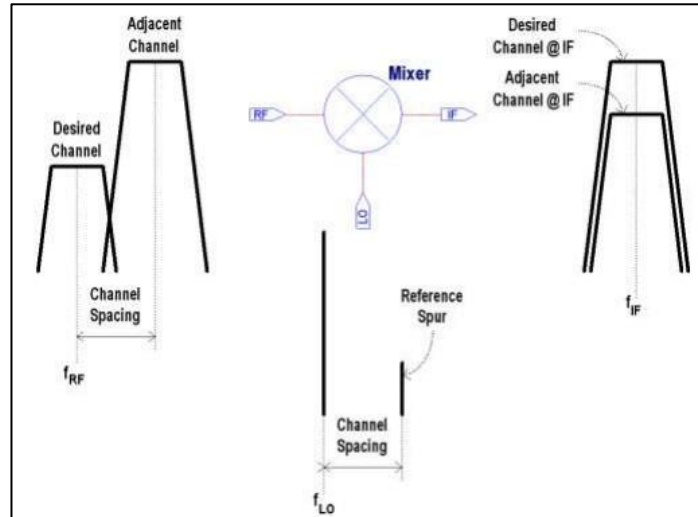


Figure 3.5: Adjacent channel interference due to reference related spur.

3.3.1. Reference Related Spurs

Reference related spurs is shown up at multiples of the comparison frequency of phase detector. Reference related spurs are based on mismatch and current leak in charge-pump. When PLL synthesizer is locked, charge pump is in tri-state. Current flow is not expected in tri-state situation. However, in reality, there exists trivial leakage current through charge pump creating modulation at the input of VCO. In today's PLL circuits, this leak current is at level of nano amps or less. Accordingly, this is not the major cause of reference related spurs. The dominant source of reference spur is due to charge pump mismatch. One of the reasons of mismatch in charge-pump is inequality between source and sink currents of the charge pump. As speed of PMOS transistor differs from that of NMOS transistor, current spikes at PFD frequency shown in Figure 3.6 [8] may give rise to modulation in VCO output [12].

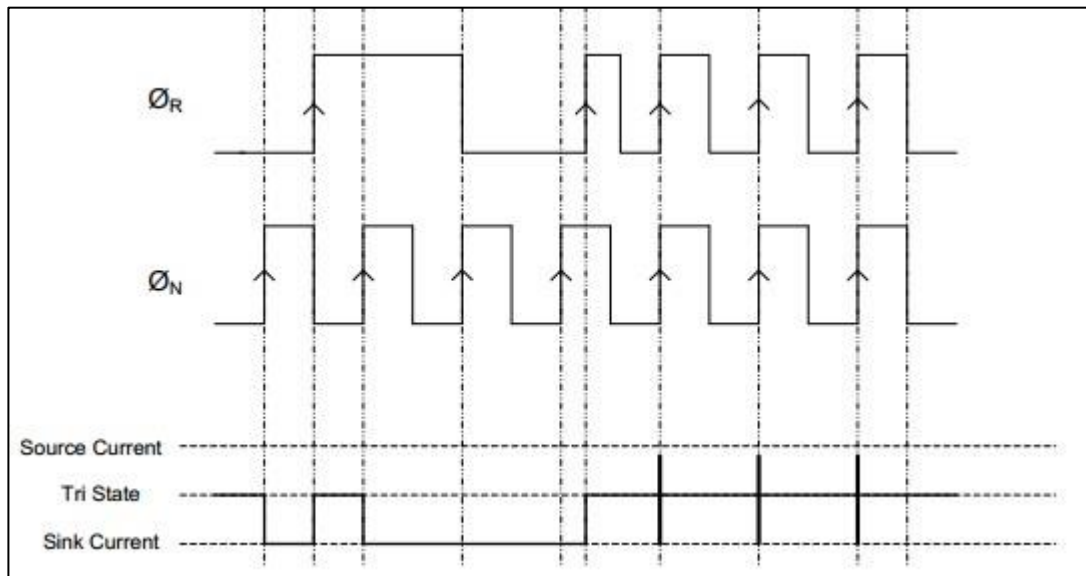


Figure 3.6: Current spikes caused by CP mismatch.

In order to send away reference related spurs from fundamental frequency synthesized, PFD frequency is selected as high as possible. Here, possibility is restricted by maximum allowed PFD frequency. Spurs are far away from corner frequency of loop filter can be filtered easily by the loop filter.

In integer-N synthesizers the step size is as PFD frequency. Therefore reference related spurs can be a problem for small step sizes. In contrast to integer-N, reference related spurs are not troublesome because step size can be decreased independently from PFD frequency.

In figure 3.7 [22], output spectrum of a frequency synthesizer with a 1 MHz PFD frequency is shown. Spurs are appeared at PFD frequency and its harmonics.

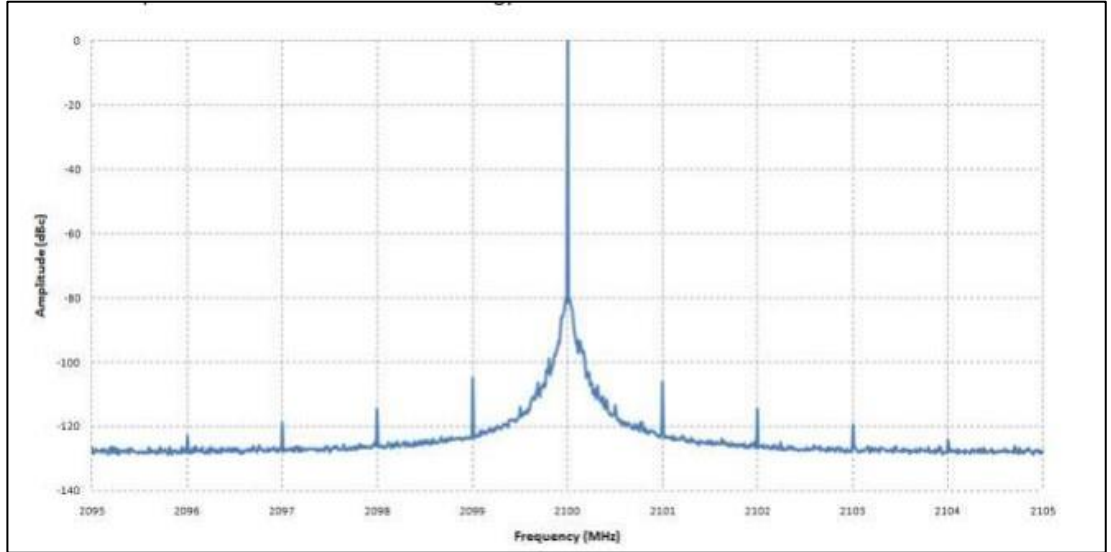


Figure 3.7: Reference related spurs at multiples of 1MHz PFD frequency.

3.3.2. Integer Boundary Spurs

Integer boundary spur (IBS) occurs due to interaction between PFD frequency and VCO output frequency or its harmonics. These spurs are observed at an offset frequency equals to difference between multiple of frequency of phase detector and frequency of VCO [11].

Once synthesizer frequency is set to close to integer multiple of frequency of phase detector, integer boundary spurs are headache [24]. This case occurs in integer-N synthesizers. In fractional-N synthesizers, synthesized frequency is generally not close to multiple of PFD frequency. Loop filter generally filters out these type of spurs in fractional-N synthesizers [8].

3.3.3. Fractional Spurs

Fractional spurs are the most troublesome spur type which appear at an offset as step size of the synthesizer from the fundamental output frequency. Fractional spurs arise from operation of accumulator or Σ - Δ modulator. To obtain an average fractional division factor, divider is changed between two or more integer values [8].

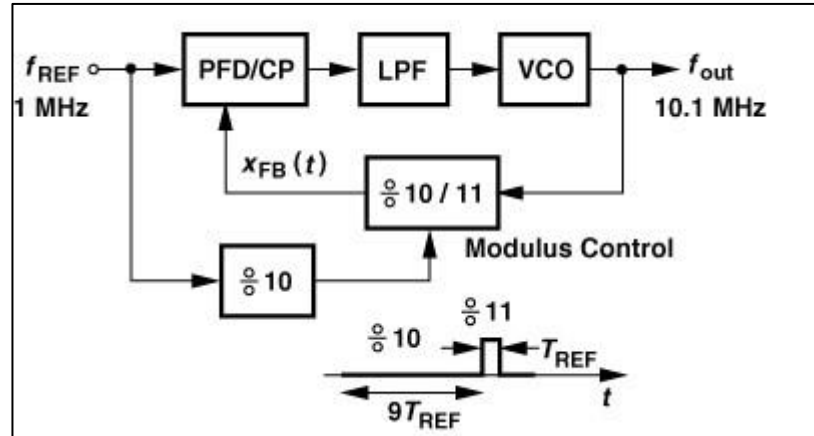


Figure 3.8: Example of fractional-N loop.

Let us examine the circuit shown in Figure 3.8[4] in time domain to understand fractional spur mechanism. Output period is equal to $(10.1 \text{ MHz})^{-1} \approx 99 \text{ nsec}$. As seen from Figure 3.8, this output period is multiplied by 10 for nine cycles of reference signal while it is multiplied by 11 for one cycle of reference signal. Duration of first nine cycle is 990 ns long which is shorter than period reference signal. The phase difference between feedback signal and reference signal increases until it becomes zero phase error, once division ratio is 11. This leads phase detector to generate wider pulse which appear as periodic waveform after loop filter. This periodic waveform is repeated in every 10 cycles of reference signal which modulates VCO at a rate of 0.1 MHz that generates spurs at offset of $\pm 0.1 \text{ MHz}$ and its harmonics from 10.1 MHz carrier frequency [4].

When channel spacing (step size) is too small, spurs fall into loop BW which are not able to be eliminated by the loop filter and they are observed within the output spectrum. To reduce the amplitude of fractional spurs, dithering method and increasing Σ - Δ order discussed in setion 3.2.1 can be utilized [8].

3.4. Phase Noise Phenomenon in Frequency Synthesizers

Ripple in amplitude and phase give rise to noise in oscillators. Output signal is given by,

$$V(t) = [V_o + \alpha(t)] \times \cos(\omega_o t + \Phi(t)) \quad (3.11)$$

where $\alpha(t)$ denotes the amplitude ripple and $\Phi(t)$ states the phase noise [7]. In most oscillators, there are amplitude limiting mechanism. Therefore amplitude fluctuation causing noise in amplitude can be ignored. Phase noise dominates the oscillator output noise [25]. Phase noise can be characterized as random phase fluctuations and is stated as,

$$V(t) = V_o \times \cos(\omega_o t + \Phi(t)) \quad (3.12)$$

A RF transceiver system is remarkably influenced by RF synthesizer performance used as local oscillator in that transceiver. Every component in frequency synthesizer contribute to overall phase noise of the synthesizer. Noise contribution can be modelled as illustrated in Figure 3.9 [7].

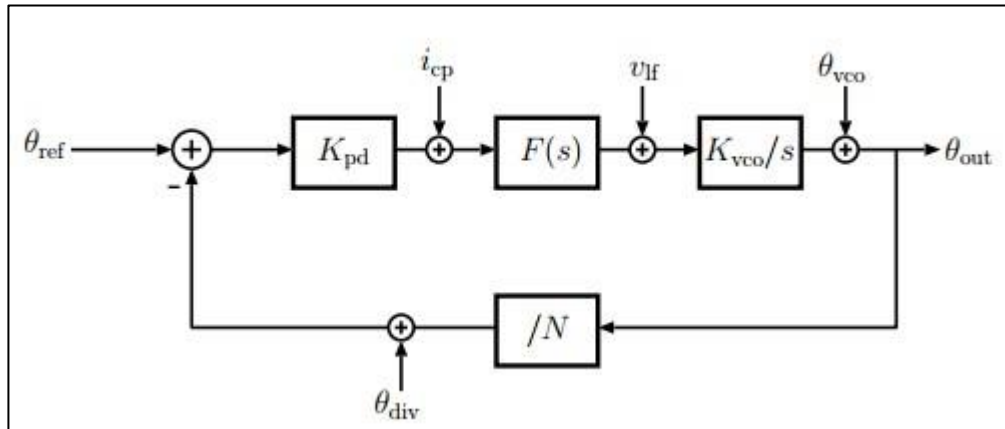


Figure 3.9: Linear phase noise model of a PLL based synthesizer.

K_{PD} is the gain phase detector and charge pump which is given by $I_{CP}/2\pi$ (A/rad) where I_{CP} is charge-pump current. K_{VCO}/s is the transfer function of the VCO

where K_{VCO} is the gain of the VCO. The loop filter transfer function is given by $F(s)$ and $1/N$ is the transfer function for frequency divider [7].

Phase noise model shown in Figure 3.9, phase noise is joint to the component output signal. Phase noise contribution is given by θ_{ref} , θ_{VCO} and θ_{div} for reference, VCO and divider, respectively. V_{lf} represents loop filter voltage noise and i_{cp} gives charge pump current noise [7]. The open loop transfer function $T_{OL}(S)$ for PLL is stated as,

$$T_{OL}(S) = \frac{K_{PD}K_{VCO}F(s)}{sN} \quad (3.13)$$

Considering individual noise contribution of PLL components, transfer function for each noise source is acquired. In this context, transfer function of the reference noise source is expressed as,

$$\begin{aligned} T_{REF}(S) &= \frac{\theta_{out}}{\theta_{ref}} = \frac{\frac{K_{PD}K_{VCO}F(s)}{s}}{1 + \frac{K_{PD}K_{VCO}F(s)}{Ns}} \\ &= N \frac{T_{OL}(S)}{1 + T_{OL}(S)} \end{aligned} \quad (3.14)$$

Current noise transfer function of the charge pump is given by,

$$\begin{aligned} T_{CP}(S) &= \frac{\theta_{out}}{i_{cp}} = \frac{\frac{K_{VCO}F(s)}{s}}{1 + \frac{K_{PD}K_{VCO}F(s)}{Ns}} \\ &= \frac{N}{K_{PD}} \cdot \frac{T_{OL}(S)}{1 + T_{OL}(S)} = N \cdot \frac{2\pi}{I_{CP}} \cdot \frac{T_{OL}(S)}{1 + T_{OL}(S)} \end{aligned} \quad (3.15)$$

Noise transfer function for the loop filter is stated by,

$$\begin{aligned} T_{LF}(S) &= \frac{\theta_{out}}{v_{lf}} = \frac{\frac{K_{VCO}}{s}}{1 + \frac{K_{PD}K_{VCO}F(s)}{Ns}} \\ &= \frac{K_{VCO}}{s} \cdot \frac{1}{1 + T_{OL}(S)} \end{aligned} \quad (3.16)$$

Relating to VCO noise transfer function, it can be expressed as,

$$T_{VCO}(S) = \frac{\theta_{out}}{\theta_{VCO}} = \frac{1}{1 + \frac{K_{PD}K_{VCO}F(s)}{Ns}} = \frac{1}{1 + T_{OL}(S)} \quad (3.17)$$

(3.16) gives the transfer function of feedback frequency divider noise.

$$T_{DIV}(S) = \frac{\theta_{out}}{\theta_{div}} = \frac{-\frac{K_{PD}K_{VCO}F(s)}{s}}{1 + \frac{K_{PD}K_{VCO}F(s)}{Ns}} = -N \frac{T_{OL}(S)}{1 + T_{OL}(S)} \quad (3.18)$$

It is seen from equations above, to obtain low phase noise at the output, low VCO gain (K_{VCO}), low division ratio (N) and high charge pump current are required. However, this parameters are selected depending on application specifications [7]. Total noise can be obtained by RMS sum of the individual noise of each component as given in (3.19) [7].

$$\begin{aligned} \theta_{out}^2 &= [\theta_{ref} \cdot T_{REF}(S)]^2 + [\theta_{div} \cdot T_{DIV}(S)]^2 + [i_{cp} \cdot T_{CP}(S)]^2 \\ &\quad + [\theta_{VCO} \cdot T_{VCO}(S)]^2 + [v_{lf} \cdot T_{LF}(S)]^2 \\ &= \left(\frac{T_{OL}(S)}{1 + T_{OL}(S)} \right)^2 \left[(N \cdot \theta_{ref})^2 + (N \cdot \theta_{div})^2 \right. \\ &\quad \left. + \left(i_{cp} \cdot N \cdot \frac{2\pi}{I_{CP}} \right)^2 \right] + \left(\frac{1}{1 + T_{OL}(S)} \right)^2 \left[\left(v_{lf} \cdot \frac{K_{VCO}}{s} \right)^2 + \theta_{VCO}^2 \right] \end{aligned} \quad (3.19)$$

It can be concluded from (3.16), phase noise of reference, phase frequency detector combined with charge pump (PFD/CP) and divider is effective at low offset frequencies, while phase noise of the VCO and loop filter is effective at high offset frequencies. Reference source, divider and PFD/CP dominant noise contributors within the loop bandwidth. In contrast, VCO dominates the phase noise outside the loop bandwidth [7].

3.4.1. Determining Optimum Loop Bandwidth For A PLL Frequency Synthesizer

Loop bandwidth is one of the significant parameters for a PLL based RF synthesizer. Phase noise of the RF synthesizer is characterized by loop filter. While VCO noise is dominant after corner frequency of the loop filter, reference, divider and phase detector noise dominate the phase noise before corner frequency which means inside loop filter. Therefore, optimum loop bandwidth is the intersection point of VCO phase noise graph and noise floor of the other noise sources such as reference, PFD and N divider. As illustrated in Figure 3.10, loop BW is selected smaller or bigger than intersection point, there probably will be performance degradation [8].

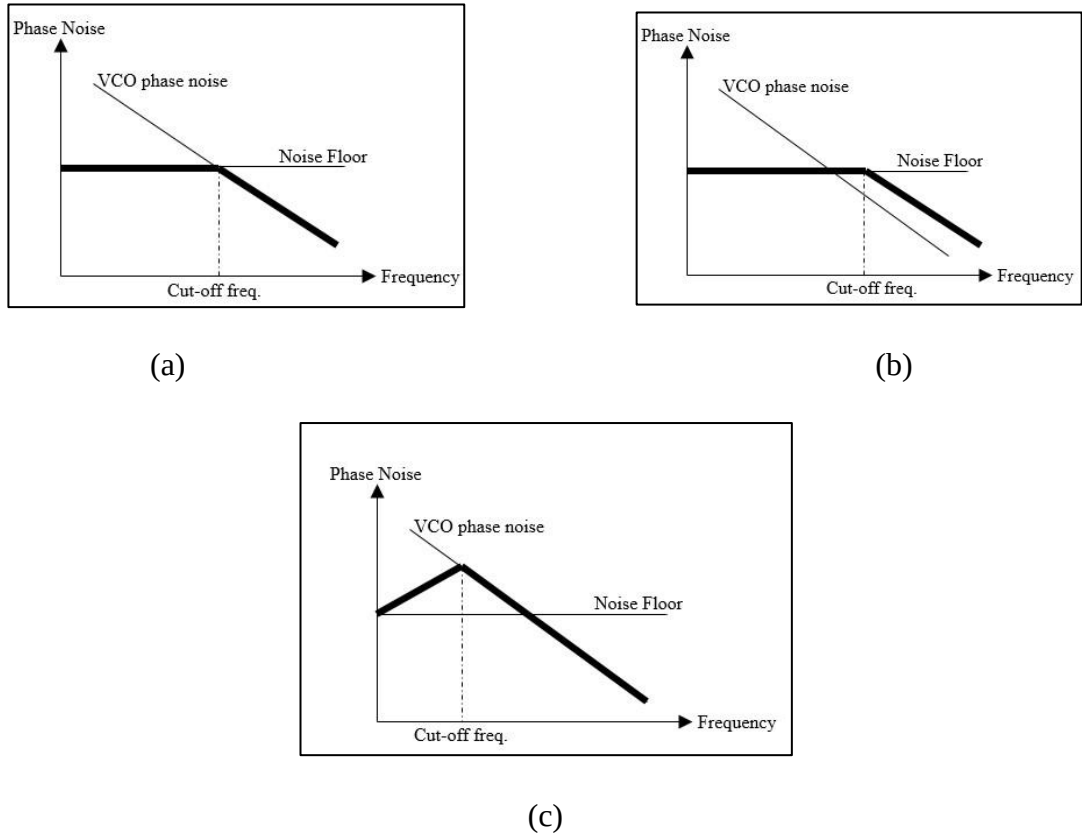


Figure 3.10: (a) optimum loop BW (b) after intersection (c) before intersection.

3.4.2 Phase Noise Prediction For A PLL Frequency Synthesizer

Phase noise value can be defined as noise ratio in a 1-Hz bandwidth at a certain frequency offset as illustrated in Figure 3.11 [1]. In a PLL system, each noise source contributes to output noise in different region. Noise of reference input is effective at the region up to 1 kHz offset frequency. In range of 1 kHz and cut-off frequency, frequency divider noise and PFD integrated with charge pump noise are dominant. After cut-off frequency, VCO noise is dominant. Noise floor is formulated as,

$$\mathcal{L}_O = 10 \log(f_{PFD}) + \mathcal{L}_{PLL} + 20 \log(N) \left[\frac{dBc}{Hz} \right] \quad (3.20)$$

where $\mathcal{L}_O$ is the noise floor, $\mathcal{L}_{PLL}$ stands for the noise of PLL circuitries, and f_{PFD} is the comparison frequency of PFD [8].

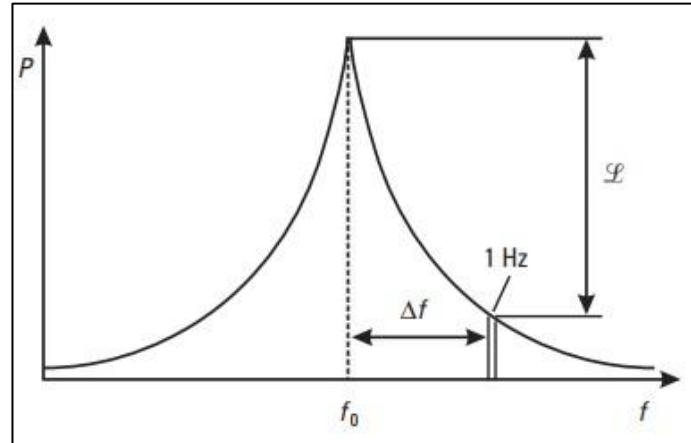


Figure 3.11: Phase noise illustration.

3.4.3 Phase Noise Improvement in PLL Frequency Synthesizers

There are some rule of thumbs to improve the phase noise at the output of the RF synthesizer. To reduce the phase noise within the loop bandwidth, first, highly clean reference source should be used. Reference phase noise will be amplified by $20\log(N/R)$. N states feedback division ratio while R is reference frequency division ratio. PFD frequency is obtained by f_{REF} / R [1], [24].

Second, PFD frequency should not to be selected too high or low, an optimum value should be selected. If low PFD frequency is used, N division ratio increases and this degrades the phase noise as $20\log N$. If high PFD frequency is chosen to use, it deteriorates the phase noise as $10\log(f_{\text{PFD}})$ [1], [8], [24], [27].

Third, In integer-N PLL, channel spacing is assigned by PFD frequency. When high resolution integer-N frequency synthesizer is intended, PFD frequency needs to be used as step size which requires high division ratio giving rise to degradation in phase noise as $20\log N$. A fractional-N architecture should be preferred in high resolution frequency synthesizer design [1], [24].

Fourth, loop bandwidth optimum value should be chosen as shown in Figure 3.10. If it is selected too narrow, VCO phase noise degrades the close-in phase noise. When loop BW is chosen too wide, PLL internal phase noise will be extended far from the carrier frequency [8], [24].

Lastly, VCO which possesses the low phase noise is chosen to improve the phase noise outside the loop BW [24].

A curve of the main contributors for output phase noise is demonstrated in Figure 3.12 [24].

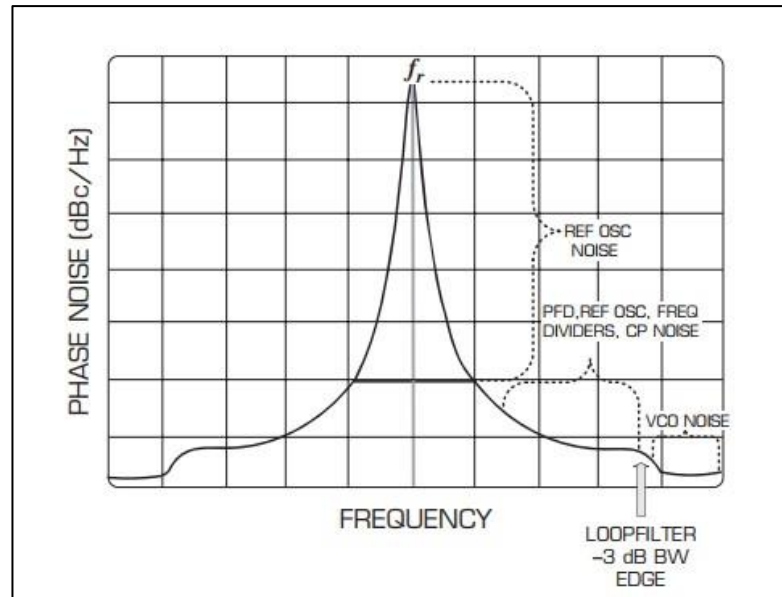


Figure 3.12: Phase noise contributors and their effective regions.

4. DESIGN OF PLL-BASED RF SYNTHESIZER

An RF synthesizer is designed to be used in an S band (2 GHz – 4GHz) receiver as a local oscillator. Diagram of the receiver is as given in Figure 4.1.

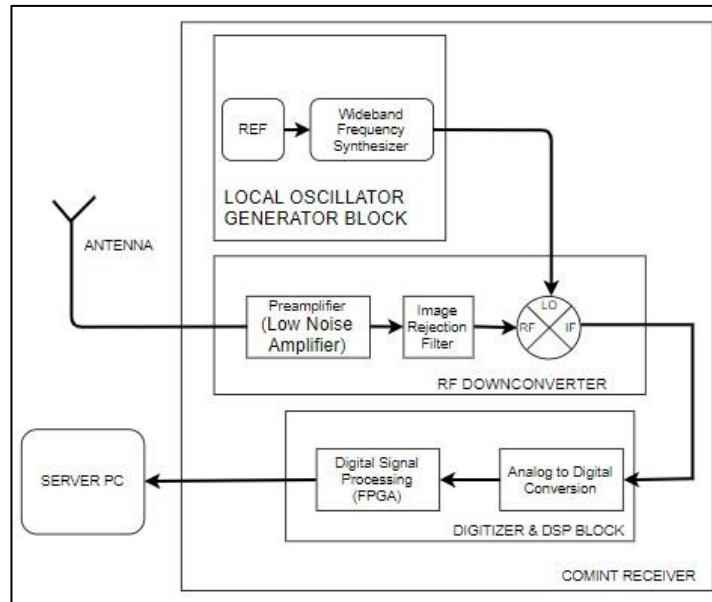


Figure 4.1: Conceptual diagram of S-band COMINT receiver.

In this chapter, components composing the purposed PLL based frequency synthesizer, simulation before implementing frequency synthesizer as a product, calculating loop filter components, designing frequency synthesizer and measurements for the implemented frequency synthesizer are discussed.

4.1. Frequency Synthesizer IC Overview

ADF5355 which is ultra wideband frequency synthesizer IC with integrated VCO of Analog Devices is utilized in designing and implementing of the PLL based RF synthesizer. Figure 4.2 illustrates functional block diagram of ADF5355 [19]. ADF5355 includes all PLL unit inside a single package except for loop filter. For flexibility of tuning loop bandwidth loop filter is outside the chip.

ADF5355 IC supports implementation of both integer-N and fractional-N architectures. VCO which is integrated to ADF5355 synthesizer IC operates in

frequency range of 3400 MHz – 6800 MHz and by means of output frequency divider and doubler, it is able to be extended to the range from 54 MHz to 13600 MHz with very high resolution. ADF5355 IC has two RF output channels. Channel A outputs 54 MHz – 6800 MHz band while channel B generates frequencies from 6800 MHz to 13.6 GHz. In this study, ADF5355 is configured to generate frequencies between 2070 MHz and 4070 MHz with 100 kHz resolution. With such LO (local oscillator), receiver can receive signals in S-band and downconvert it to 70 MHz IF (intermediate frequency).

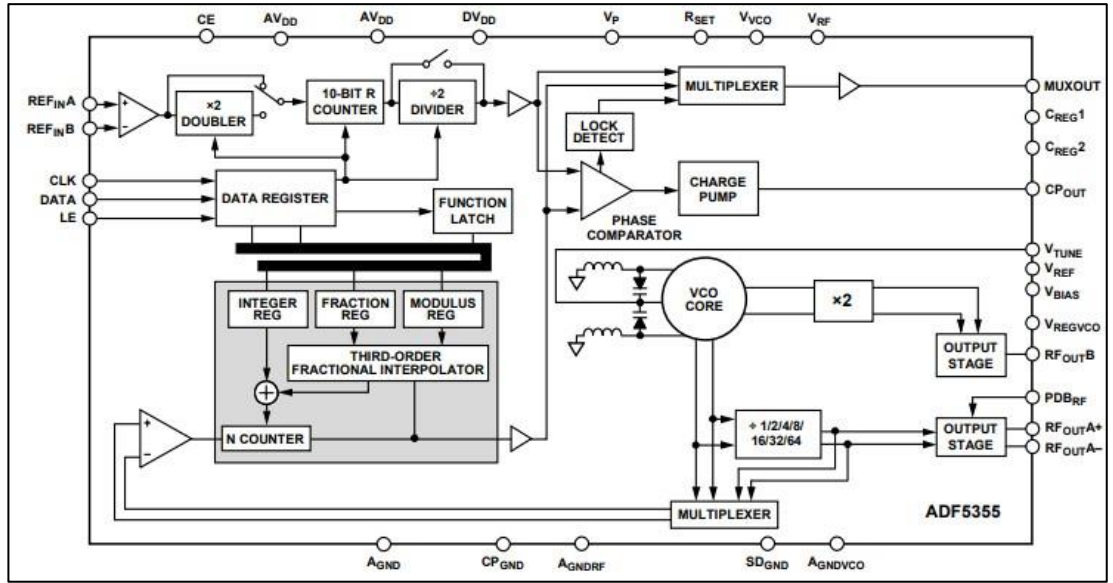


Figure 4.2: Functional block diagram of ADF5355 synthesizer IC.

4.1.1. Reference Input Circuitry

ADF5355 IC accepts both differential and single-ended reference signal. This can be configured by software over serial peripheral interface (SPI). Designed and implemented synthesizer utilizes single-ended configuration because reference crystal oscillator has single-ended output.

Reference input circuitry includes reference frequency doubler and divider block (Div) composed of 10-bit R counter and divide-by-2 sub-units. Reference doubler is used to double the reference frequency to improve phase noise and spurious performance of PLL frequency synthesizer module. Divider blocks can be utilized when, integer-N architecture is preferred to generate a frequency in order to

acquire low channel spacing. However this configuration degrades phase noise by $20\log(\text{Div} \times f_{\text{VCO}} / f_{\text{REF}})$. In this application, doubler is enabled while reference division factor is one which means no division for reference signal frequency. By doubling 10 MHz reference frequency, 20 MHz PFD frequency is utilized for comparison. Thus, it is purposed to improve phase noise by some amount.

4.1.2. Phase-Frequency Detector and Charge Pump Circuitry

ADF5355 includes a PFD circuitry integrated with a charge pump. In PFD/CP circuitry has a delay element which prevents dead zone issue causing reference related spurs. A simplified block diagram of PFD/CP circuitry is illustrated in Figure 4.3 [19].

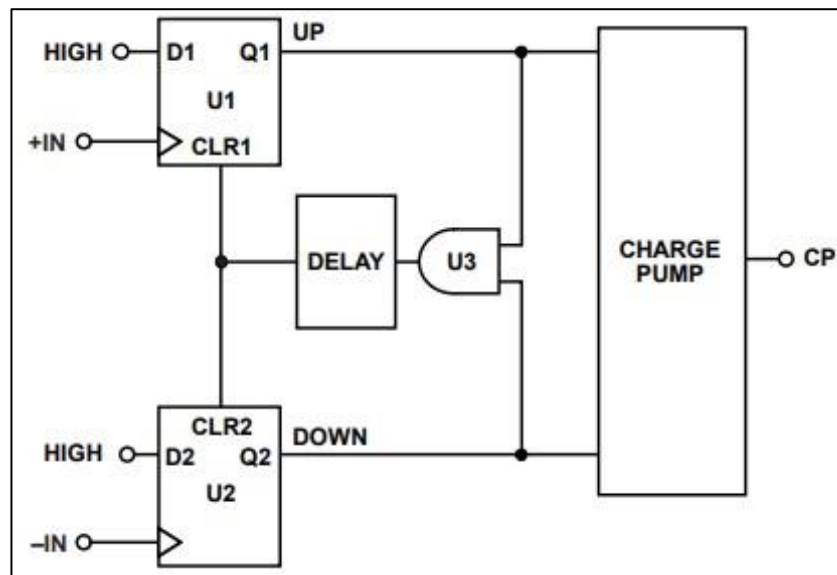


Figure 4.3: Functional block diagram of ADF5355 PFD/CP circuitry .

4.1.3. Loop Filter Circuitry

Loop filter circuitry is installed between charge pump output pin and tuning voltage input of ADF5355 synthesizer chip. A third order low pass filter is designed and implemented as loop filter. Components which build loop filter is calculated by a simulator is published by Applied Radio Labs. Simulator gives frequency and time domain responses such as phase error, closed loop gain, phase margin, locking time

and so on. Simulation results and loop filter values for components will be given in the following sections.

One of the main advantage of ADF5355 is loop filter type. When discrete VCO is used for such wideband application, tuning voltage, required for used frequency range, exceeds the charge pump upper limit and there an active filter with an amplifier need to be used. Using amplifier in loop filter circuit contributes to overall phase noise and consumes more power [26].

4.1.4. VCO and Output Stage Circuitry

ADF5355 has a VCO core which consists of four separate VCOs, thus, it is able to cover a wide range with small VCO sensitivity (K_{VCO}). VCO core covers frequency range from 3400 MHz to 6800 MHz. Other frequency values are able to generate using output divider and doubler integrated to ADF5355 IC. VCO phase noise is given in Figure 4.3 [19].

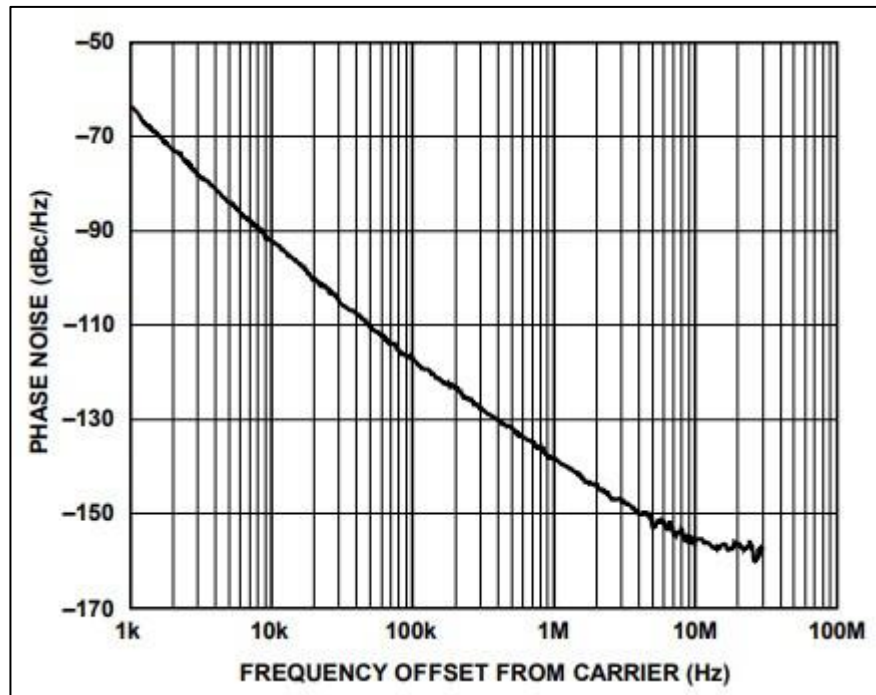


Figure 4.4: Open loop phase noise of ADF5355 internal VCO at 3.4GHz.

ADF5355 has two RF output channels, channel A and channel B. In design, channel A is used for outputting synthesized frequency. Channel B is terminated by 50Ω terminator.

VCO is connected to channel A output stage through a buffered output divider. Output divider has ability to divide the VCO frequency by 1, 2, 4, 8, 16, 32 and 64. In this design, target frequency range is from 2070 MHz to 4070 MHz. Division ratio is 1 from 3400 MHz to 4070 MHz while it is 2 from 2070 MHz to 3400 MHz. Division ratio is programmed over SPI interface.

Channel A is employed by an NPN differential pair. Output A+ and A- is taken from the collectors of the transistors and biased through 50Ω from RF power supply (V_{RF}) which is +3.3VDC, typically. ADF5355 has four different power level configuration, -4dBm, -1dBm, +2dBm, +5dBm. Power level is able to programmed via SPI interface. Output stage is as shown in Figure 4.5 [19].

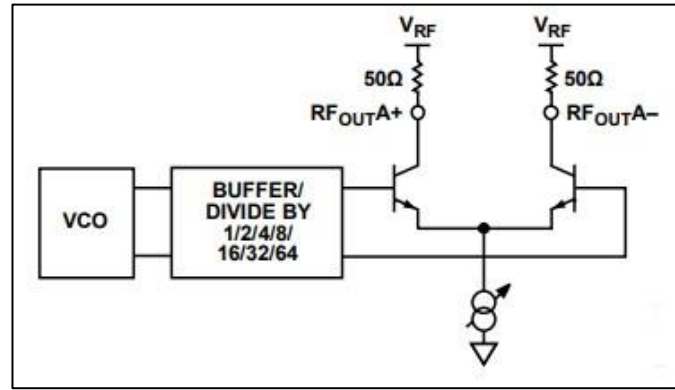


Figure 4.5: ADF5355 output stage.

4.1.5. RF Feedback Divider Circuitry

ADF5355 includes third-order Σ - Δ modulator in N divider circuitry. N value is determined by dual modulus prescaler (P/P+1) and INT (integer), FRAC1, FRAC2 (fraction), MOD1, MOD2 (modulus) counter values. With this divider, ADF5355 can exhibit good noise performance and high resolution ability. N divider functional block diagram is shown in Figure 4.6 [19]

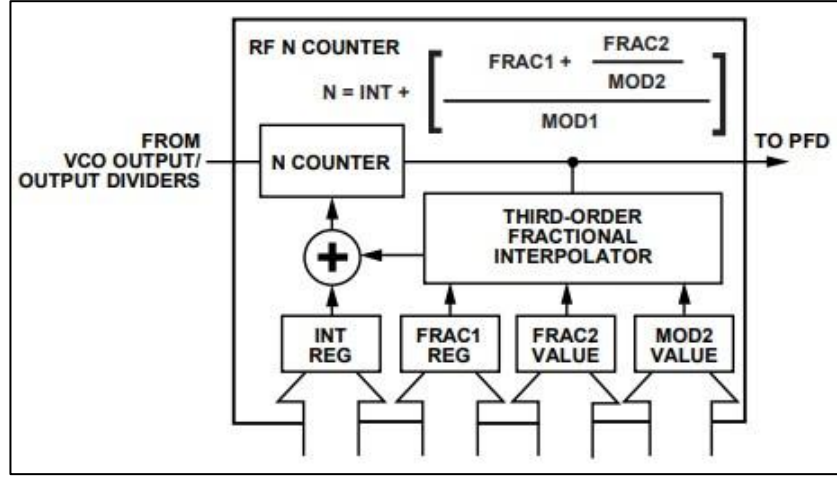


Figure 4.6: N Divider functional block diagram.

4.1.5.1. Calculation of N Divider Parameters

Output frequency is given by,

$$f_{VCO_{OUT}} = N \times f_{PFD} \quad (4.1)$$

where VCO_{OUT} is fundamental (no output division used) output frequency of VCO. N is embodied by,

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \quad (4.2)$$

INT is 16-bit value. It is between 23 and 32767 if dual modulus prescaler is (P/P+1) 4/5, 75 and 65535 if dual modulus prescaler is 8/9. FRAC1 is the numerator of 24-bit primary modulus. It can be set from 0 to 2^{24} . FRAC2 is the numerator of 14-bit secondary modulus MOD2 is programmable 14-bit modulus and MOD1 is a constant 24 bit modulus (2^{24}). INT can be obtained by integer part of fractional N division factor. INT and other counter values are as given in (4.3), (4.4), (4.5) and (4.6).

$$INT = int(N) \quad (4.3)$$

$$FRAC1 = \text{int}[(N - INT) \times MOD1] \quad (4.4)$$

$$MOD2 = \frac{f_{PFD}}{GCD(f_{PFD}, f_{step})} \quad (4.5)$$

GCD stands for the greatest common divisor.

$$FRAC2 = [(N - INT) \times MOD1 - FRAC1] \times MOD2 \quad (4.6)$$

4.2. Simulation of PLL Frequency Synthesizer

Simulations are realized using ADISimPLL software which is a trademark of Applied Radio Labs v5.00. Abracon's 10 MHz OCXO is used as reference source of the synthesizer. Table 4.1 illustrates specifications of the OCXO [28].

Table 4.1: Specifications for 10 MHz OCXO.

Supply Voltage	+3.3 VDC typ.
Power Consumption	3W @startup, 1W @steady state
Daily Aging	±1.0 ppb
Frequency stability vs. Supply Voltage	±5.0 ppb
Offset:	Phase Noise:
1 Hz	-90 dBc/Hz
10 Hz	-120 dBc/Hz
100 Hz	-140 dBc/Hz
1 kHz	-145 dBc/Hz
10 kHz	-150 dBc/Hz
100 kHz	-155 dBc/Hz

Phase noise of the reference source simulated in ADISimPLL is as illustrated in Figure 4.7.

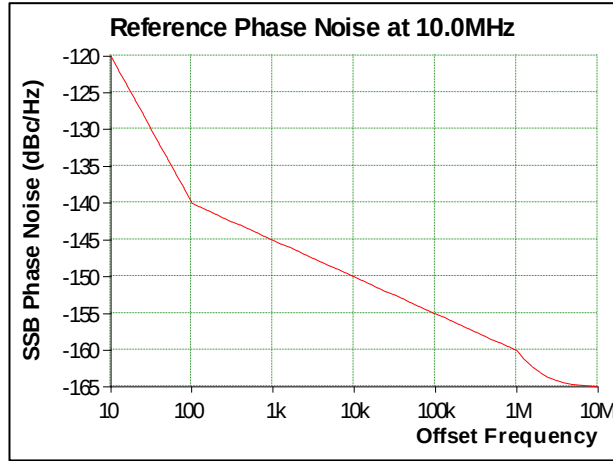


Figure 4.7: Simulated phase noise for OCXO.

ADF5355 uses its internal VCO core to generate an output signal. VCO core covers fundamentally a range of 3400 MHz – 6800 MHz. Sensitivity of integrated VCO is 15 MHz/V in average. Open loop phase noise at 100kHz offset for 4070 MHz which is within synthesizer operating band (2.07 GHz to 4.07 GHz) is approximately -114 dBc/Hz. Open loop phase noise of VCO which is simulated by ADISimPLL is given in Figure 4.8 [19].

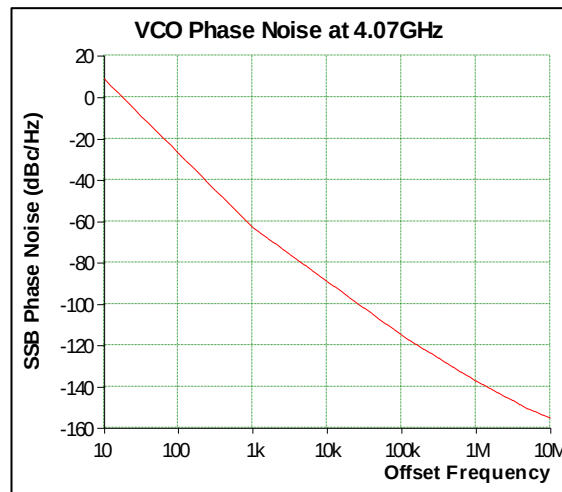


Figure 4.8: Phase noise of VCO at 4.07 GHz.

Integrated VCO has 9 pF tuning port input capacitance and it is supplied by +5 VDC (V_{VCO}) [19].

4.2.1. Determination of Loop Bandwidth

Loop filter is simulated and optimized for different loop BW and phase margin. Simulation results are compared to one another. Phase noise values for varied loop bandwidth is illustrated in Figure 4.9. As discussed in previous chapters, phase noise participation of phase frequency detector, charge-pump and frequency dividers reduce outside the loop BW while noise contribution of VCO is effective. Hence, as loop bandwidth is designed to be narrower, overall phase noise performance approaches to VCO phase noise performance. This results in degradation in close-in phase noise.

Locking time is also closely related to loop bandwidth. The narrower loop bandwidth it is designed, the longer we get locking time. ADF5355 performs automatic calibration for integrated VCO which takes approximately 2884 us with timeout values for the fastest calibration [19]. The locking time and calibration duration determines the overall locking time for the synthesizer. Locking time is also simulated by means of ADISimPLL software. All simulations are done for 4070 MHz.

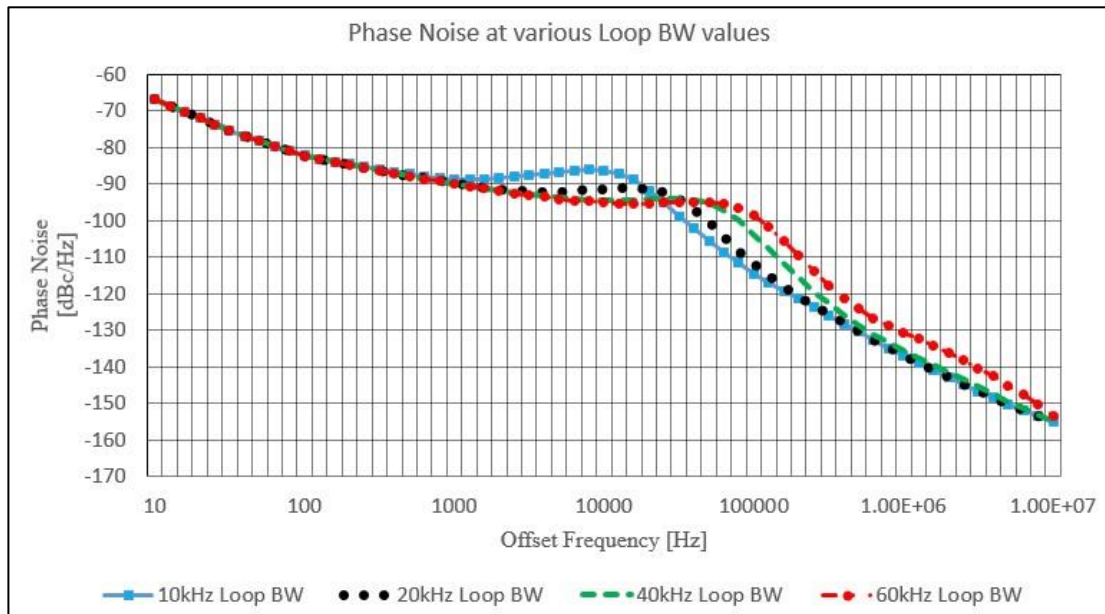


Figure 4.9: Phase noise at different loop BWs.

As seen from Figure 4.9, as loop bandwidth gets narrow, the phase noise approaches to that of VCO. On the other hand, as loop BW widens, PFD, CP and

divider noises stretch to higher offset frequency. As a conclusion, narrower BW degrades close-in noise while it improves noise at higher offset frequencies. Keeping all these facts in view, 20kHz is evaluated as optimum value for the loop BW. Beside of phase noise, locking time for different loop BW value is tabulated in Table 4.2.

Table 4.2: Frequency switching time at various loop BW.

Loop Bandwidth	Lock Time
10 kHz	3.23 msec
20 kHz	3.06 msec
40 kHz	2.98 msec
60 kHz	2.96 msec

Phase margin is related to the stability of the loop. It is appropriate to choose it between 40° and 55° . Simulations demonstrate that the optimum locking time is obtained at phase margin range between 40° and 55° . While loop BW is fixed at 2 kHz, switching time at different phase margin values is listed in Table 4.3.

Table 4.3: Frequency switching time at different phase margin.

Phase Margin	Lock Time
80°	No lock
65°	3.29 msec
55°	3.09 msec
45°	3.06 msec
40°	3.10 msec
35°	3.12 msec
25°	3.24 msec

While realizing loop filter whose circuitry is shown in Figure 4.10, standard capacitor and resistor values need to be used. Therefore non-standard values are optimized to these standard values.

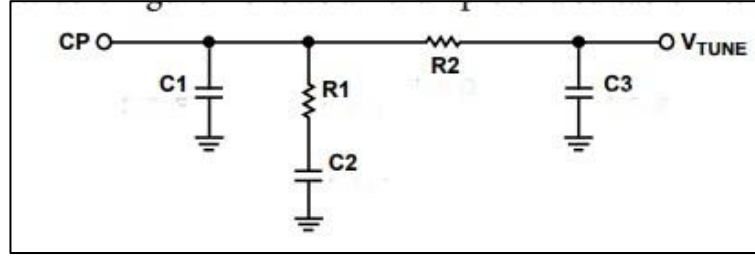


Figure 4.10: Purposed 3rd order loop filter circuitry.

After optimization, new loop bandwidth and phase margin are as given in Table 4.4.

Table 4.4: Loop BW and phase margin for calculated and used filter components.

Component	Calculated	Used
C1	714 pF	820 pF
R1	2.29 k Ω	1.8 k Ω
C2	9.72 nF	12 nF
R2	4.69 k Ω	4.7 k Ω
C3	317 pF	270 pF
Loop BW	20 kHz	19.8 kHz
Phase Margin	45°	48°

4.2.2. Characteristics of PLL Frequency Synthesizer

Simulation of transient frequency error, transient phase error, transient phase characteristics, open loop gain, closed loop gain and phase noise performance of the proposed frequency synthesizer with standard component values is performed and examined.

Simulated frequency synthesizer schematic is illustrated in Figure 4.11. Loop bandwidth and phase margin can be observed from open loop gain simulation result given in Figure 4.12(a). As discussed in previous chapters, phase noise of the reference, PFD with charge pump and feedback divider is multiplied by closed loop gain and transferred to the output. Outside the loop BW, VCO dominates the output phase noise performance. Closed loop gain plot is as shown in Figure 4.12(b).

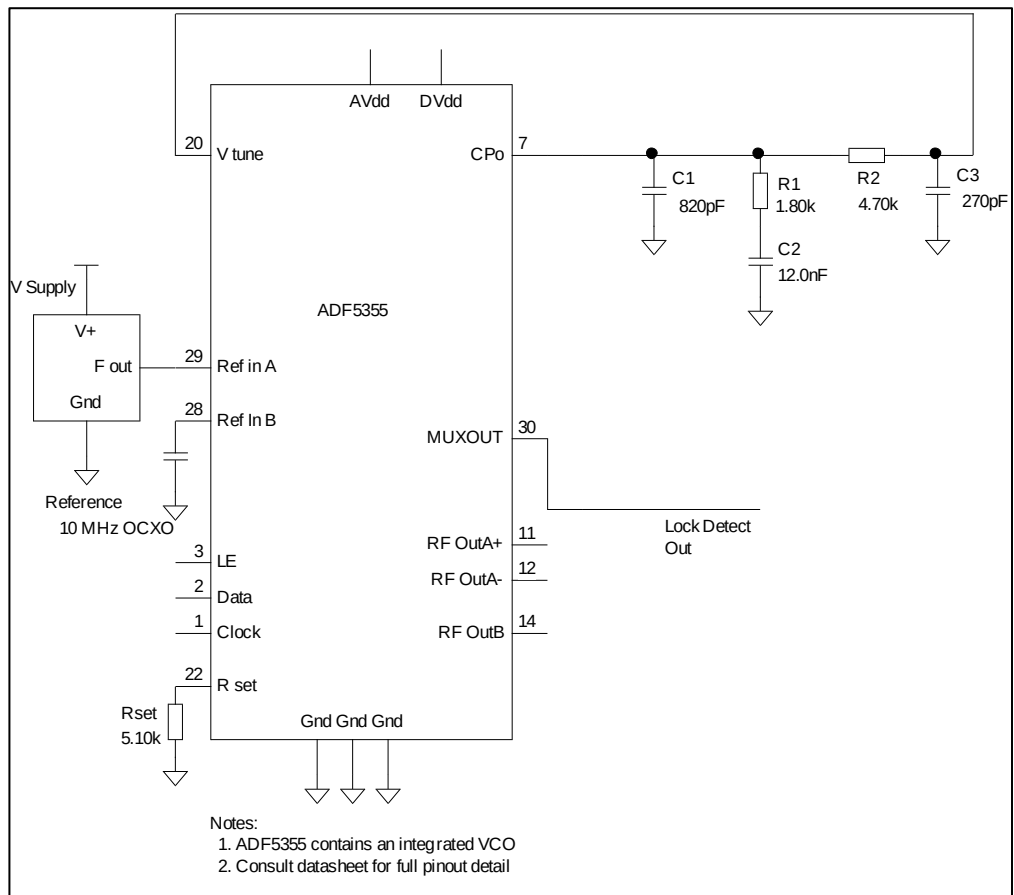
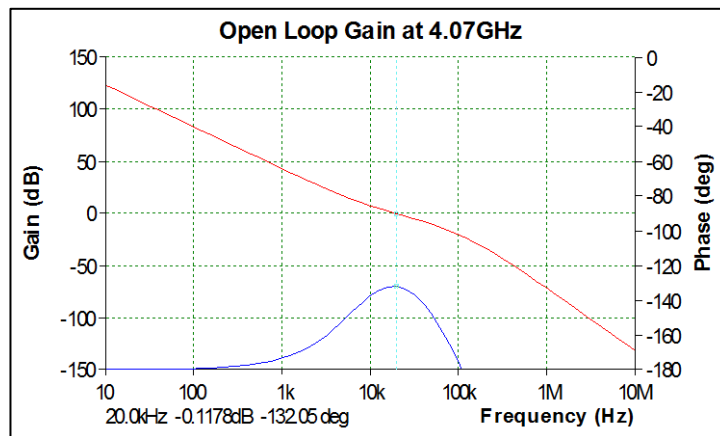
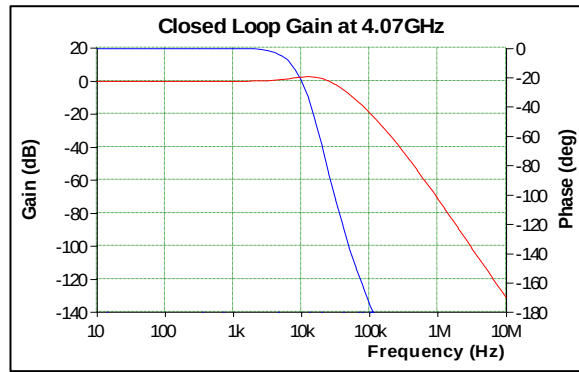


Figure 4.11: Simulated schematics of ADF5355 synthesizer.



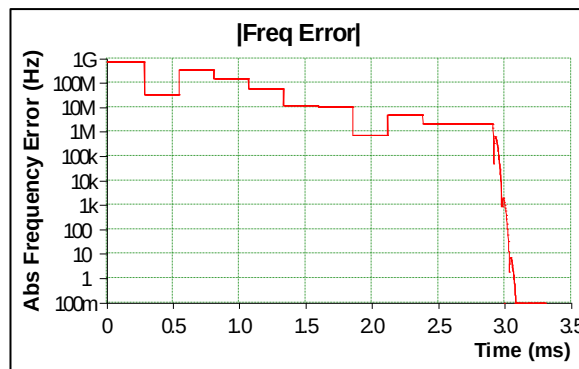
(a)



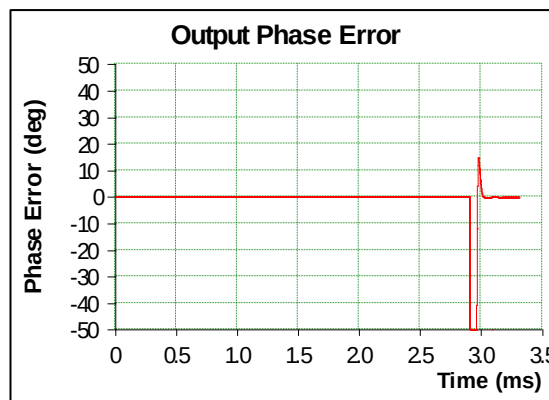
(b)

Figure 4.12: (a) open loop gain (b) closed loop gain of proposed PLL system.

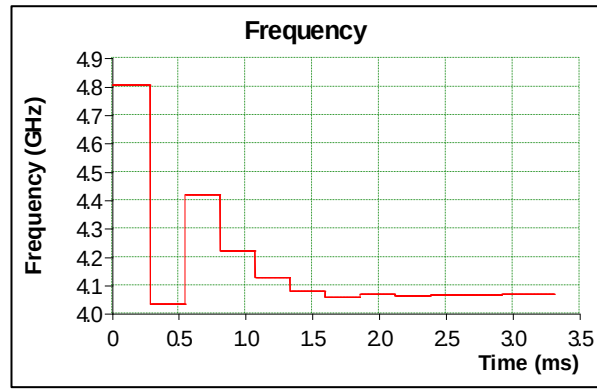
Open loop gain approximately 0dB and phase margin 48° at 19.8 kHz. Figure 4.13 (a), (b) and (c) shows synthesized frequency error, output phase error and frequency characteristics, respectively.



(a)



(b)



(c)

Figure 4.13: (a) frequency error (b) phase error while (c) frequency characteristics.

4.2.3. Phase Noise Simulation

Simulations show that noise of reference input dominates the phase noise characteristics up to loop bandwidth and VCO starts to dominate the phase noise performance after the loop bandwidth as it is expected. Overall phase noise response after offset of 20 kHz follows the VCO noise. This result is as expected which discussed in previous chapters. Overall phase noise at various offset shown in Figure 4.14.

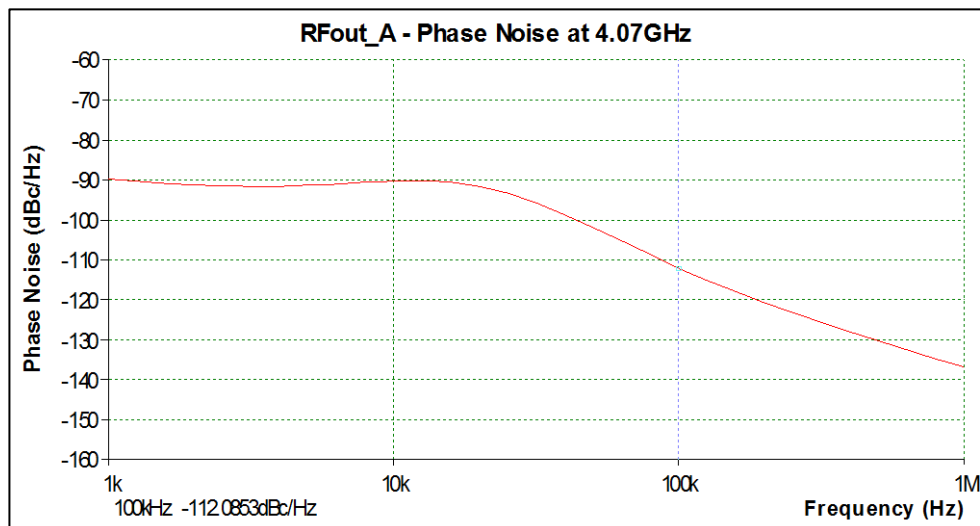


Figure 4.14: Simulated phase noise response at 4070 MHz.

When output frequency is reduced by keeping the other settings fixed, phase noise is changed by $20\log N$. When simulation is repeated with 2070 MHz RF_{OUT} , simulation result is as shown in Figure 4.16 along with . As expected it is improved by $20\log (4070/2070) \approx 6$ dB.

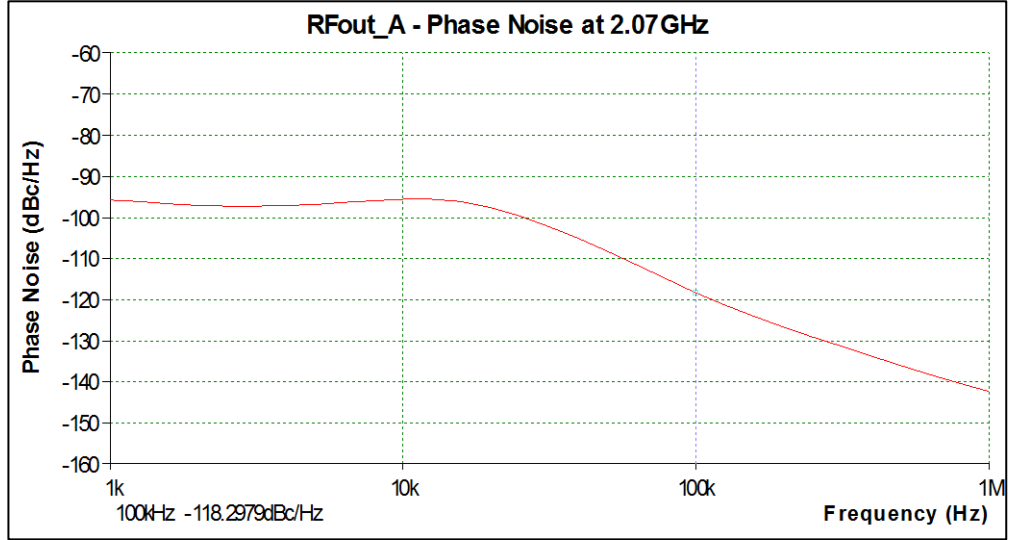


Figure 4.15: Simulated phase noise response at 2070 MHz.

4.3. Design and Implementation

In this section, detailed information about design and implementation of PLL based frequency are given. Design consideration for power, analog, RF and digital circuitries are discussed and implemented at design phase.

KiCad which is open source schematic and PCB design tool is used to draw schematic and board. KiCad is very practical tool for board prototyping. Being priceless and practical to use makes it encouraging to choose over other CAD tools.

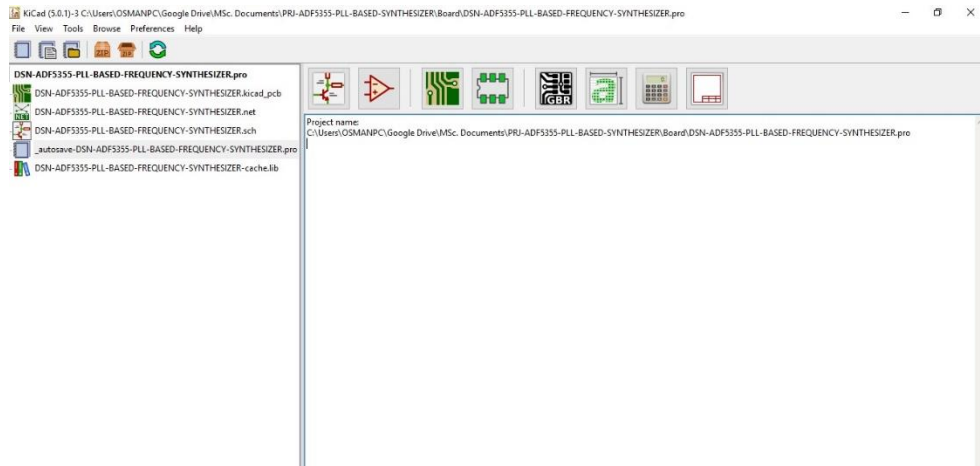


Figure 4.16: KiCad along with project navigator and toolbars

4.3.1. Board Material

PCB is the environment to that all synthesizer circuits are implemented. There are different kind of material for PCBs. The material of two-layer PCB is FR-4 for this design. It is preferred because it can be easily found at low prices. Thickness of the board is 0.8 mm. The copper thickness is 1 oz (35 μm).

4.3.2. Design Method For PLL Circuits

Main component of the designed and implemented frequency synthesizer board is ADF5355 wideband frequency synthesizer integrated circuit. Excluding loop filter, all PLL components such as PFD, charge-pump, reference divider and doubler, VCO and feedback divider is integrated within a single chip. ADF5355 has 32-lead LFCSP package with size of 5 mm x 5mm [19].

Because PLL circuit is an RF based circuit, care is taken for impedance matching issue. PCB material is FR-4 and characteristic impedance calculation is realized so that it can be matched to 50 Ω . There are four RF lines which are subjected to this requirement: Channel A+, channel A-, channel B and reference input line. For calculations, a free tool called AppCAD by Avago is used. AppCAD needs some parameter related to line whose impedance is calculated. This parameters are line width (W), distance between RF line and reference ground plane underneath, copper thickness, gap between RF line and ground plane on same layer with RF line

and dielectric constant of the PCB material. Grounded coplanar waveguide (GCPW) structure achieving good isolation is used for RF transmission lines. AppCAD calculation is illustrated in Figure 4.17.

Ground vias nearby RF line is placed properly for better isolation and phase noise performance. DC blocking capacitors are placed on RF lines. Π -type attenuators are also placed onto RF lines to be able to adjust signal amplitude. In this design only one of the RF lines is used hence, other two RF channels are terminated by a $50\ \Omega$ in series with a DC blocking capacitor.

Loop filter circuit should be considered to be placed close to V_{TUNE} pin of ADF5355. This is an important consideration in terms of noise coupling to the tuning line of VCO.

AppCAD - [CPW]

File Calculate Select Parameters Options Help

Coplanar Waveguide ☒ With Groundplane ☐ No Groundplane

Calculate Z0 [F4]

Diagram parameters: L=100, H=0.8, T=0.035, W=1, G=0.3

Dielectric: $\epsilon_r = 4.6$ (FR-4)

Frequency: 4 GHz

Length Units: mm

Calculated results:

- $Z_0 = 50.3\ \Omega$
- Elect Length = 2.262 λ
- Elect Length = 814.2 degrees
- Elect Length = 169.504 mm (Air Line equiv.)
- Delay = 565.404 ps
- 1.0 Wavelength = 44.216 mm
- $V_p = 0.590$ fraction of c
- $\epsilon_{eff} = 2.87$
- Shape factor = 0.625

Normal Click for Web: APPLICATION NOTES - MODELS - DESIGN TIPS - DATA SHEETS - S-PARAMETERS

Figure 4.17: AppCAD tool $50\ \Omega$ RF line calculation.

4.3.3. Design Method For Power Supply Circuits

RF frequency synthesizer board is supplied by +6 V DC power supply. ADF5355 IC is supplied by three low noise regulators. ADF5355 includes different type of circuitries inside such as analog, RF and digital circuitries. These circuitries

should be supplied for better noise performance. Therefore three different regulators are used. While analog supply (A_{VDD}) and digital supply (D_{VDD}) are supplied by two separate 3.3 V regulators, charge-pump (V_P) and VCO (V_{VCO}) are supplied by single 5 V regulator.

Power supply noise can effect the phase noise performance of the synthesizer. In this context, ADM7151 low noise and high PSRR low dropout regulator is used to implemet these power supply circuitries. Care should be taken for low noise design. Power supply filtering with capacitors and ferrite beads should be implemented carefully. Placement of power decoupling capacitors correctly. These bypass capacitors should be placed close to ADF5355 IC. +5 V regulator circuitry is shown in Figure 4.18.

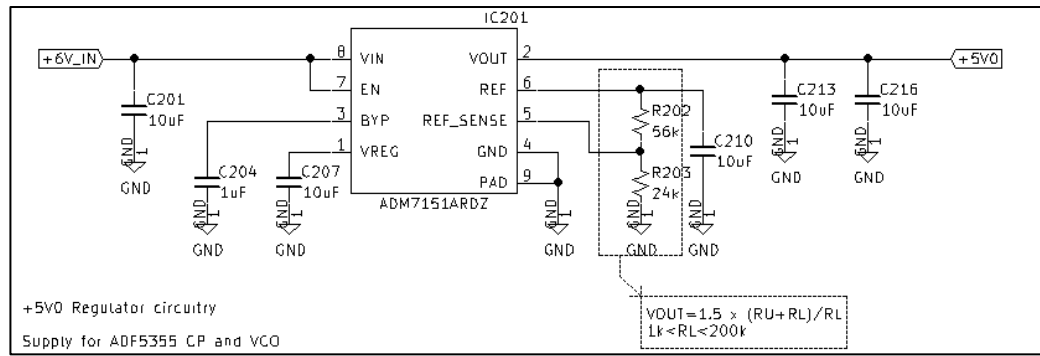


Figure 4.18: +5 V regulator circuitry.

4.3.4. Design Method For Digital Circuits

Programming ADF5355 is fulfilled over SPI which stands for serial peripheral interface. SPI is a synchronous serial protocol [1]. ADF5355 needs a master SPI driver to be programmed [19]. In this study, ATmega328P is used to configure the ADF5355 over SPI. ATmega328P is a microcontroller from 8-bit microcontroller family of Microchip Technology, Inc. MCU is not included in purposed board design. It is connected to ADF5355 board externally. Logic inputs of ADF5355 accepts signals that are between 1.5 V and 3.3 V as logical high. To map the output signal level of MCU in between 1.5 V ~ 3.3 V, a resistor divider network is used.

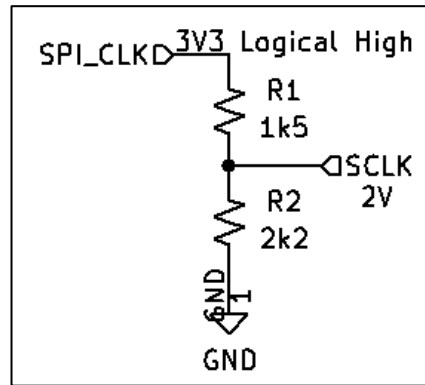


Figure 4.19: SPI signal level translation.

SPI clock frequency is chosen as 500 kHz. This is able to be configured by software in coding phase. Commercial central control unit (MCU) is shown in Figure 4.20.



Figure 4.20: ATmega328P based Arduino Nano board.

4.3.5. Implementing Frequency Synthesizer

In KiCad, board schematic is drawn in two separate sheets. One includes power subsystem and the other includes RF subsystem with ADF5355 IC. Schematics are shown in Figure 4.21 and 4.22.

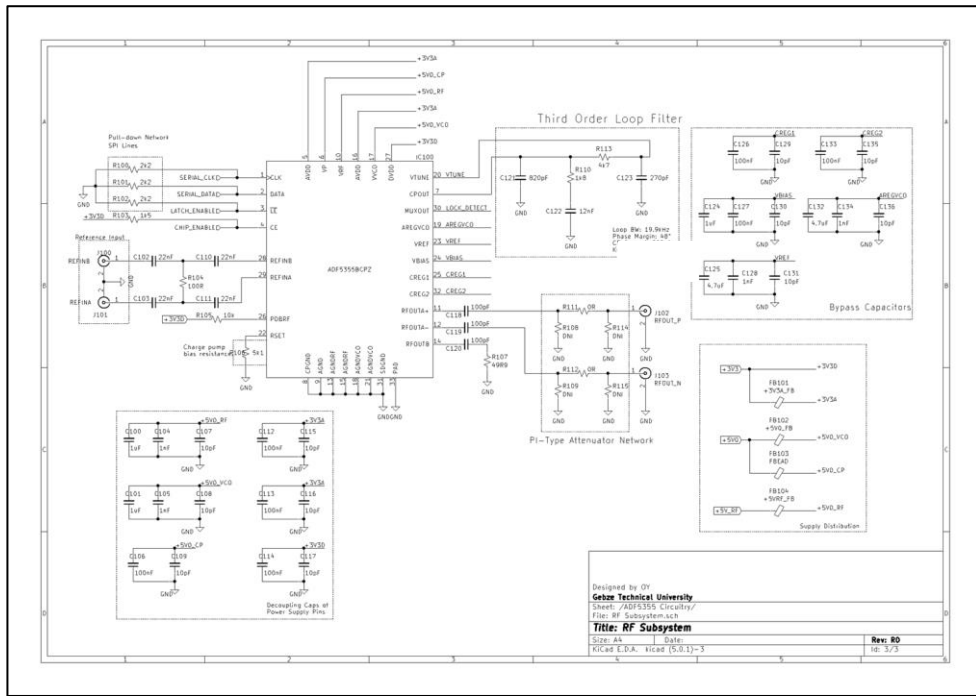


Figure 4.21: RF subsystem schematics.

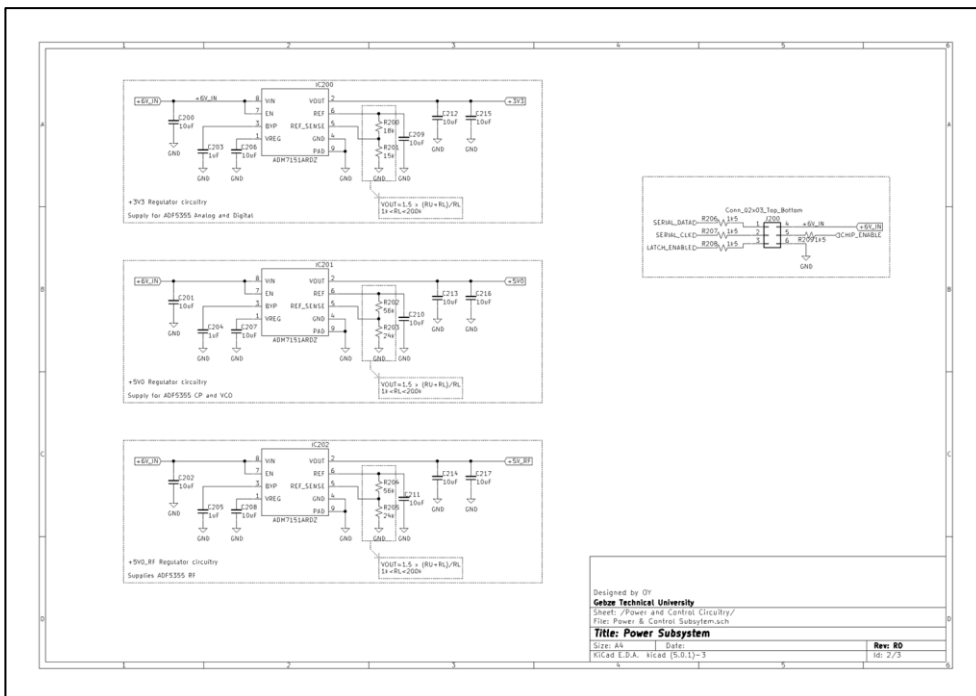


Figure 4.22: Power subsystem schematics.

Synthesizer is referenced by Abracon's 10 MHz OCXO whose output level is +2 dBm. DC blocking capacitor is used in reference signal line. OCXO is not in the board design, it is used as external reference.

10 kHz third order loop filter is used between CP output pin and VCO tuning pin. Phase margin is selected as 45° but implemented loop filter by standard commercial values gives 2.2 kHz loop bandwidth and 46.5° phase margin.

There are fixed attenuator network on output lines. By means of attenuators, output signal level can be fixed at desired value which is below default output amplitude of ADF5355 IC.

4.3.6. Configuring Operation Parameters

Synthesizer is programmed over SPI interface. Using SPI interface, registers of ADF5355 is set. For, 10 MHz reference frequency and 20 MHz PFD frequency

$$F_{PFD} = F_{REF} \times \left[\frac{1 + D}{R \times (1 + T)} \right] \quad (4.7)$$

Reference doubler is enabled which means D bit is 1. R counter value is 1 and divide-by-2 is disabled that means T is 0. The desired $F_{PFD} = 20$ MHz and $F_{REF} = 10$ MHz values are obtained by this configuration. To get 4070 MHz output frequency with 100kHz channel spacing, desired parameters are calculated as follow. Calculations is performed by using equation (4.3).

$$INT = \text{int} \left(\frac{4070}{20} \right) = 195$$

$$FRAC1 = \text{int} \left[\left(\frac{4070}{20} - 195 \right) \times 2^{24} \right] = 8,388,608$$

$$MOD2 = \frac{20000 \text{ kHz}}{GCD(20000 \text{ kHz}, 100 \text{ kHz})} = 200$$

$$FRAC2 = [(203.5 - 203) \times 2^{24} - 8,388,608] \times 200 = 0$$

Charge pump current is adjusted to 900uA and muxout function is set to digital lock detection. RF output power configured as -4 dBm.

4.3.7 Measurements

PCB design of the board is given in Figure 4.23 and 3-dimensional illustration is in Figure 4.24.

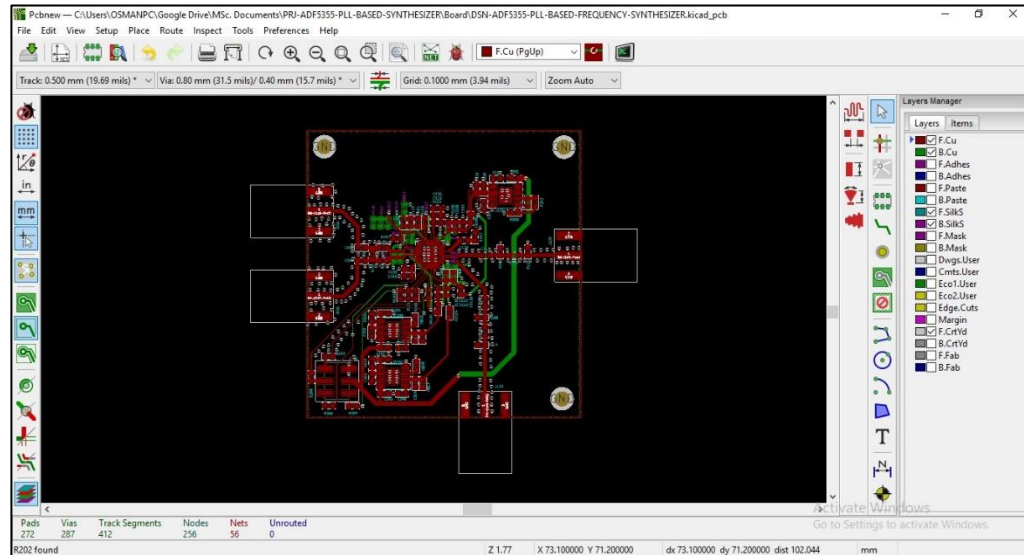


Figure 4.23: PCB drawing

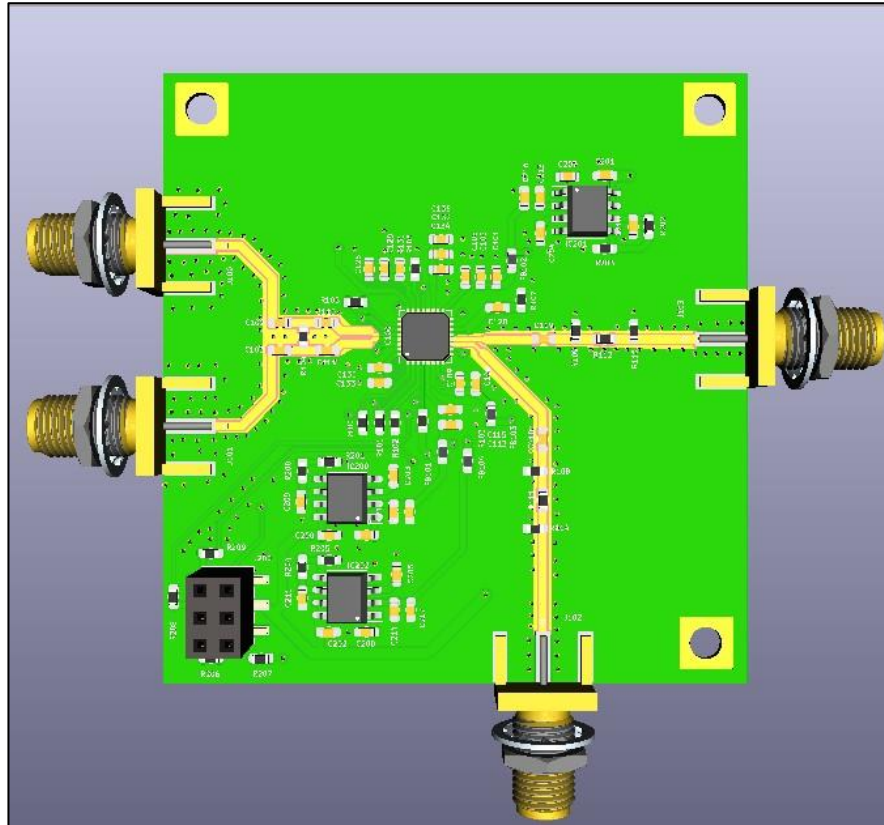


Figure 4.24: 3D illustration of frequency synthesizer.

Board is powered by Agilent E3632A DC power supply adjusted to 6V. Current drawn by board is shown in Figure 4.25.



Figure 4.25: Power supply current drawn by the board.

RF measurements are done by means of Rohde & Schwarz FSU Series spectrum analyzer. Output spectrum of frequency synthesizer is shown in Figure 4.26.

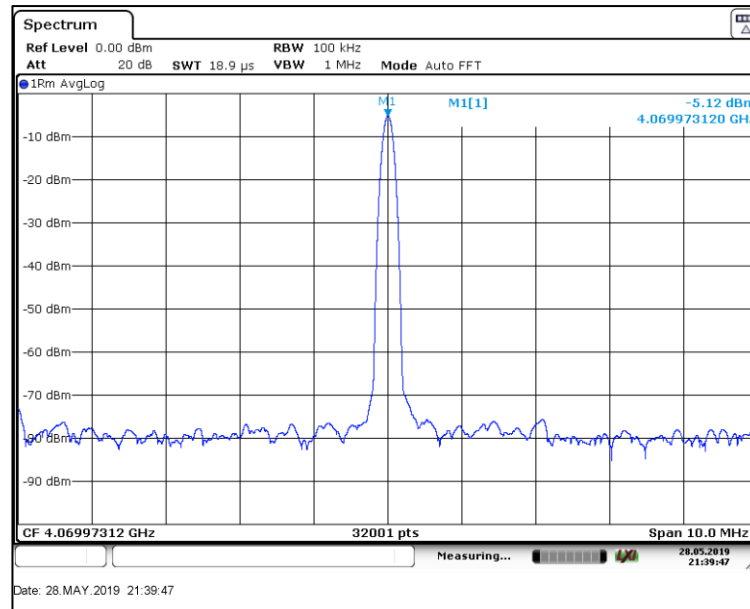


Figure 4.26: Output spectrum

Harmonic response of the synthesizer is as shown in Figure 4.27.

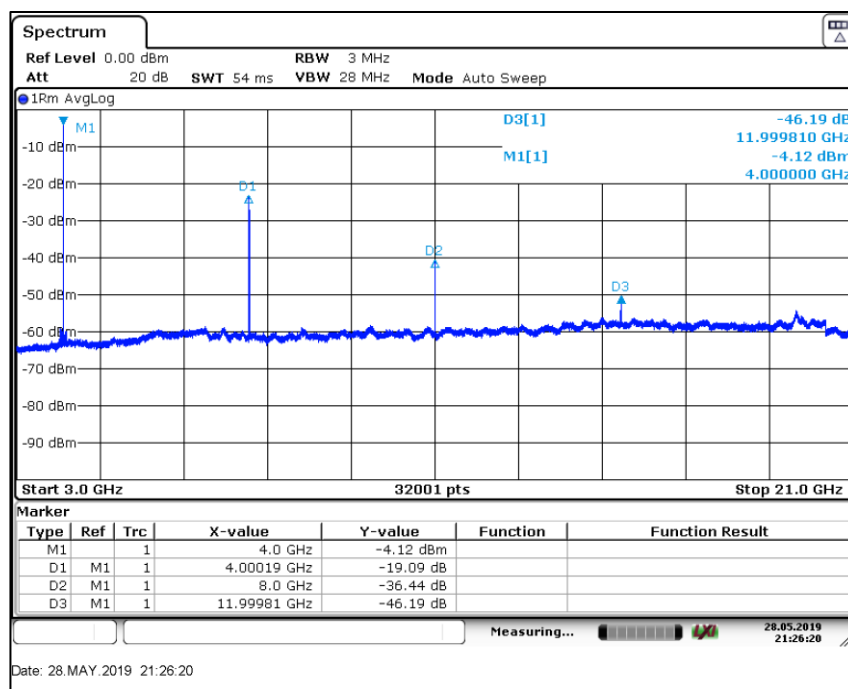
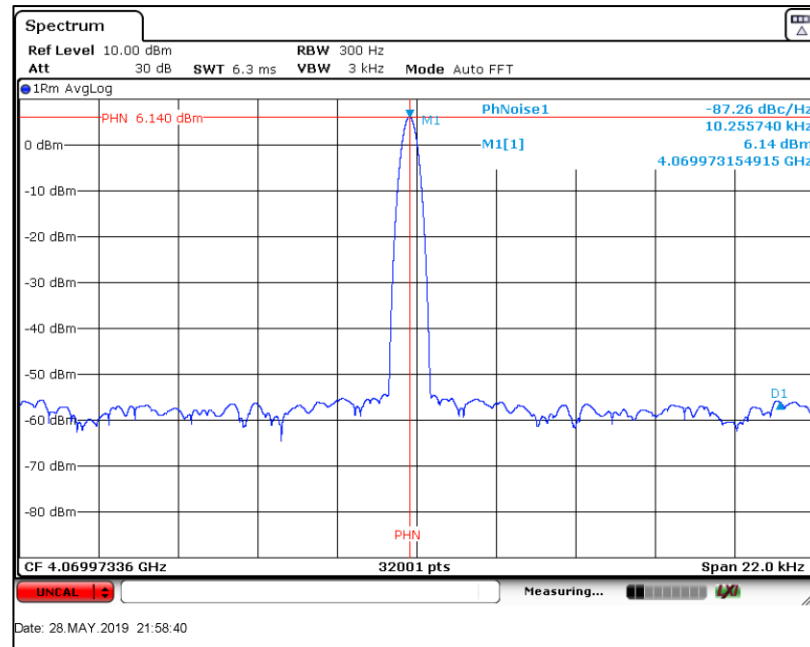
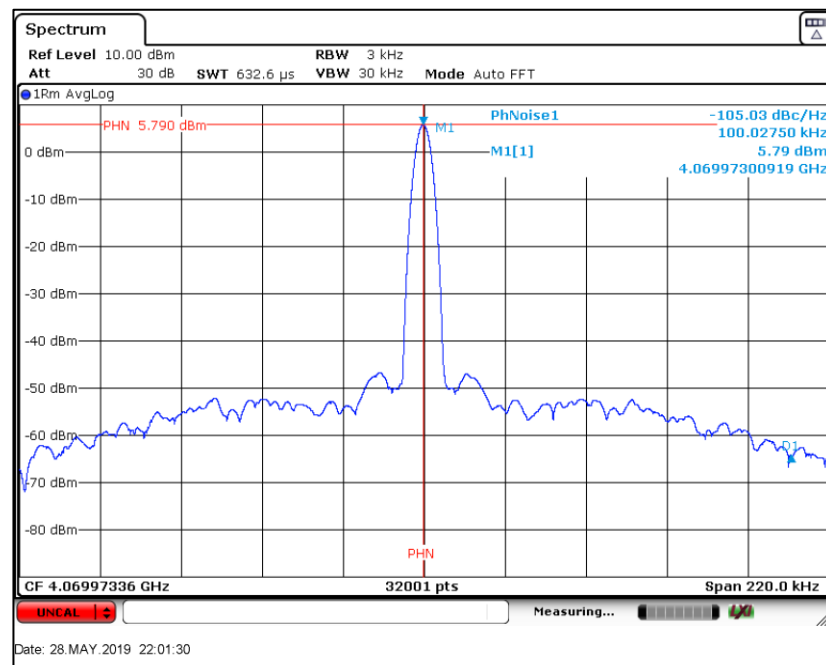


Figure 4.27: Harmonic response measurement.

Phase noise measurement is done by using phase noise measurement R&S Vector Signal Analyzer. Phase noise measurement for 4070 MHz at 10 kHz and 100kHz offsets are as shown in Figure 4.28 (a) and (b), respectively.



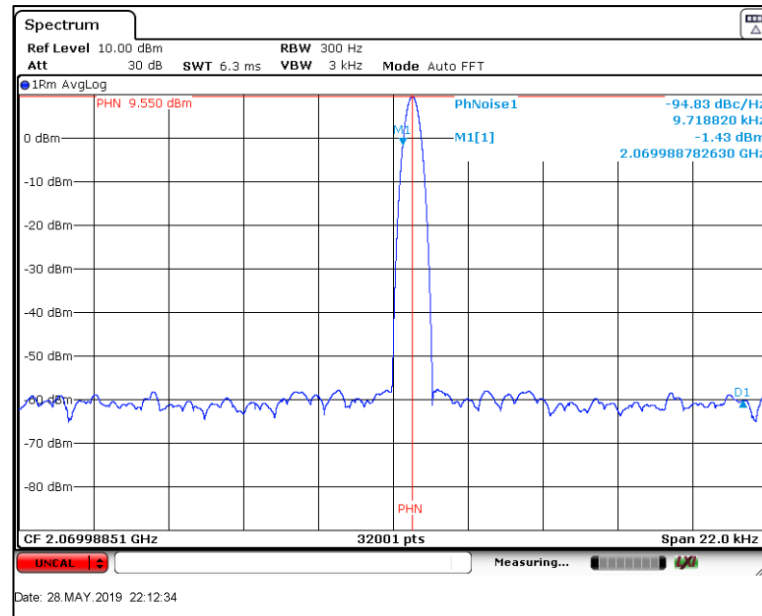
(a)



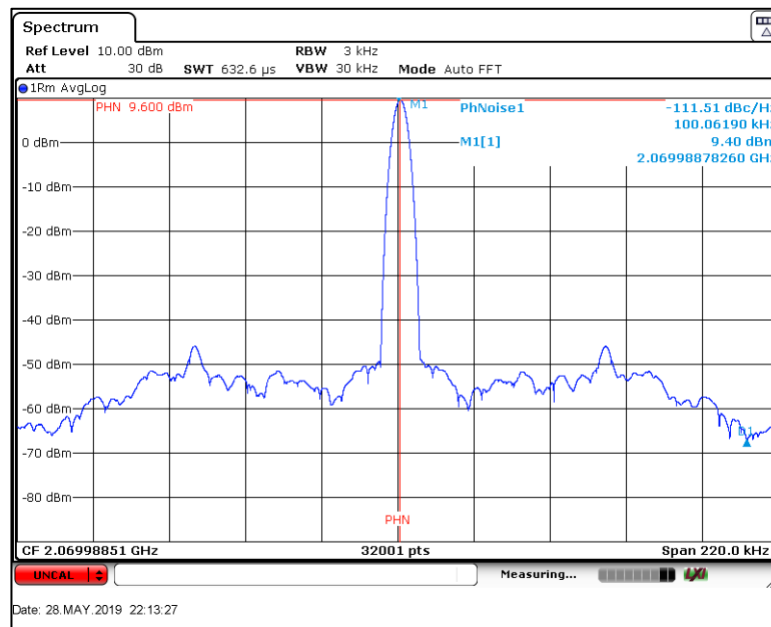
(b)

Figure 4.28: 4.07 GHz phase noise result at (a) 10 kHz and (b) 100 kHz.

To see feedback divider effect on phase noise, output frequency is changed to 2070 MHz and phase noise measurements for 10 kHz and 100 kHz offset is as shown in Figure 4.29 (a) and (b), respectively. Table 4.5 shows the results.



(a)



(b)

Figure 4.29: 2.07 GHz phase noise result at (a) 10 kHz and (b) 100 kHz.

As expected, measured phase noise is coincided with simulated phase noise. There is a few dB difference between them. The PCB material FR-4 has high dielectric constant degrading phase noise. Phase noise measurement result can be improved by using a material having less dielectric loss such as RO4003C, RO4350B and so on. In such sensitive measurements, it is likely that there are small measurement deviations.

Table 4.5: Phase noise result for 2070 MHz and 4070 MHz.

Offset (Hz)	Phase Noise (dBc/Hz)	
	4070 MHz	2070 MHz
1 kHz	-87.69	-95.26
10 kHz	-87.26	-94.83
100 kHz	-105.03	-111.51
1 MHz	-130.42	-136.90

Specifications of prototyped PLL based frequency synthesizer is tabulated in Table 4.6.

Table 4.6: Specification of the synthesizer.

Frequency Range	2.07 GHz – 4.07 GHz
Amplitude (dBm)	-5
Harmonic Level (dBc)	-15
Power Supply Voltage	+6 V
Current Consumption	223 mA
Phase Noise (dBm/Hz)	
1 kHz	-87.69
10 kHz	-87.26
100 kHz	-105.03
1 MHz	-130.42

5. CONCLUSION AND FUTURE WORKS

Phase noise is one of the most important performance indicator in communication platforms. Phase noise performance can have negative effects in the communication platform whose channel spacing is small. To get clean and stabilized oscillator in these platforms, PLL technique is used to implement frequency synthesizer. To improve phase noise performance, N value should be chosen smaller in accordance with output frequency and PFD frequency. Therefore fractional-N architecture is used to get small channel spacing while PFD is able to be high. Provided that VCO tuning voltage is not out of charge pump output range, passive filter should be chosen. Otherwise, noise of OP-AMP in active filter degrades phase noise performance. VCO should be selected to be low phase noise one. In addition, using high PSRR and low noise RF linear regulator is important for phase noise performance.

In this thesis study, a PLL based frequency synthesizer is prototyped to operate at frequency in range between 2.07 GHz – 4.07 GHz. Synthesizer is utilized as LO in an S-band receiver. Design is implemented by discrete components. A loop filter is designed and simulated to give good phase noise performance and lock time. Optimum loop bandwidth is decided to be 20kHz by means of simulations. Simulations are fulfilled by ADISimPLL simulation tool which gives results that are very close to lab. measurements. Design is done by KiCad design tool which is open source software and practical to use. Phase noise values are measured as -73 dBm/Hz at 1 kHz, -87 dBm/Hz at 10 kHz, -113 dBm/Hz at 100 kHz and -135 dBm/Hz at 1 MHz offsets. Measured noise values and simulated noise values are very close to each other, as expected. Taking into consideration that PCB material is FR-4, Using a material with lower dielectric constant such as RO4003C, RO4350B by Rogers Corporation is able to improve phase noise performance.

ADF5355 IC perform internal automatic calibration operation to select appropriate VCO and VCO subband. Automatic calibration approximately takes 2.88 msec and this result in longer lock times. Analog Devices has published an application note [29] which explains how to bypass VCO automatic calibration. This method can be added to obtain faster lock time in the future.

ADF5355 is integrated with wideband VCO core, it can be considered to design a general purpose wideband signal generator in the future. Modulation capability can be added to this general purpose generator. ASK, FSK, PSK, AM and FM modulation capabilities can be thrown in frequency synthesizer. To implement a frequency synthesizer with better phase noise performance, offset mixing technique with dual PLL stage or hybrid PLL/DDS based frequency synthesizer schemes can be used. In addition to better phase noise, this probably results in faster locking time.

REFERENCES

- [1] Chenakin A., (2010), "Frequency Synthesizers: Concept to Product", 1st Edition, Artech House.
- [2] Robins W. P., (1984), "Phase Noise in Signal Sources", Peter Peregrinus Ltd.
- [3] Desikachari R., (2003), "High Speed CMOS Dual-Modulus Prescaler for Frequency Synthesis", Master of Science Thesis, Oregon State University.
- [4] Razavi B., (2011), "RF Microelectronics", 2nd Edition, Prentice Hall.
- [5] Best R. E., (2003), "Phase Locked Loops: Design, Simulation and Applications", 5th Edition, McGraw-Hill.
- [6] Analog Devices, (2009), "Fundamental of Phase Locked Loops", Tutorial.
- [7] Kamal N., (2000), "Reference Spurs in an Integer-N Phase Locked Loop: Analysis, Modeling and Design", Doctor of Philosophy Thesis, University of Adelaide.
- [8] Bölücek M. A., (2009), "Design and Implementation of Low Phase Noise Phase Locked Loop Based Local Oscillator", Master of Science Thesis, Middle East Technical University.
- [9] Vaucher C. S., (2002), "Architectures for RF Frequency Synthesizers", Springer.
- [10] National Semiconductor, (1995), "A Fast Locking Scheme for PLL Frequency Synthesizer", Application Note.
- [11] Analog Devices, (2013), "6.2 GHz Fractional-N Frequency Synthesizer", ADF4156 Datasheet.
- [12] Banerjee D., (2006), "PLL Performance, Simulation and Design", 4th Edition.
- [13] Philips Semiconductor, (1994), "SA8025 Fractional-N Synthesizer for 2GHz Band Applications", Application Note.
- [14] Glisic S., Wolfgang W., (2006), "A Broadband Low Spur Fully Integrated BiCMOS PLL for 60 GHz Wireless Applications", 451-454, IEEE Radio and Wireless Symposium, San Diego, CA, USA, 17-19 October.
- [15] Pawar S. N., Pradeep B. M., (2017), "Wideband PLL Frequency Synthesizer: A Survey", 1-6, Mumbai, INDIA, 1-2 December.
- [16] Manthana V. K., (2011) "Ultra Low Power CMOS Phase-Locked Loop Frequency Synthesizer", Doctor of Philosophy Thesis, Nanyang Technological

University.

- [17] Egan W. F., (1999), "Frequency Synthesis by Phase Lock", 2nd Edition, Wiley & Sons Inc.
- [18] Harikrushna D., Tiwari M., Singh J. K., Khare A., (2011), "Design, Implementation and Characterization of XOR Phase Detector For DPLL in 45nm CMOS Technology", *Advance Computing: An International Journal*, 2 (6), 45 – 57.
- [19] Analog Devices, (2017), "Microwave Wideband Synthesizer with integrated VCO", ADF5355 Datasheet.
- [20] Kroupa V. F., (2003), "Phase Lock Loops and Frequency Synthesis", Wiley & Sons Inc.
- [21] Barrett C., (1999), "Fractional/Integer-N PLL Basics", Texas Instruments, Technical Brief.
- [22] Linear Technology (2013), "A Simple Method to Accurately Predict PLL Reference Spur Levels Due to Leakage Current", Application Note.
- [23] Hajimiri A., Lee T. H., (2006), "Oscillator Phase Noise: A Tutorial", *IEEE Journal of Solid-State Circuits*, 35 (3), 326-336.
- [24] Sayre C. W., (2008), "Complete Wireless Design", 2nd Edition, McGraw-Hill.
- [25] Hajimiri A., Lee T. H., (1999), "The Design of Low Noise Oscillators", Springer.
- [26] Shu K., Sinencio E. S., (2005), "CMOS PLL Synthesizer: Analysis and Design", Springer.
- [27] Yeom K. W., (2015), "Microwave Circuit Design: A Practical Approach Using ADS", Prentice Hall.
- [28] Abracon (2014), "Oven Controlled Crystal Oscillators", AOCJY2 Series Datasheet.
- [29] Analog Devices, (2018), "How to Bypass VCO Calibration for the ADF4355-2, ADF4355, ADF4355-3, ADF4356, ADF5355, and ADF5356", Application Note.

BIOGRAPHY

Osman YURDAKUL was born in Antalya in 1989. He got his bachelor degree from the Department of Electrical and Electronics Engineering of Selçuk University in 2011. He started his graduate education in the Department of Electronic Engineering at the Institute of Science and Technology of Gebze Technical University in 2016. He has worked as a hardware design engineer more than 6 years in different companies. Present, he is working at AirTies Wireless Networks as Senior Hardware Engineer.

APPENDICES

Appendix A: Publications within the Scope of Thesis

Yurdakul O., Şuvak Ö., (2019), “Determining Loop Bandwidth for Optimal Phase Noise and Locking Time Performance in PLL Based Synthesizers”, Gebze Technical University Institute of Natural and Applied Sciences, Graduate Studies Symposium & Presentation Days, 17-18 June.

Yurdakul O., Şuvak Ö., (2018), “XOR Tabanlı Faz Dedektörü İle D Flip-Flop Tabanlı Faz-Frekans Detektörünün Karşılaştırılması”, Gebze Technical University Institute of Natural and Applied Sciences, Graduate Studies Symposium & Presentation Days, 14-16 May.