

T.R.
GEBZE TECHNICAL UNIVERSITY
GRADUATE SCHOOL

GROWTH AND CHARACTERIZATION OF SINGLE CELL TiO₂
THIN FILM BASED MEMRISTIVE DEVICE

NORA ALI ABDO SALEH AL-JAWFI

A THESIS OF MASTER OF SCIENCE
DEPARTMENT OF PHYSICS

ADVISOR: ASSOC.PROF. DR. SİNAN KAZAN

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GEBZE TEKNİK ÜNİVERSİTESİ
LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

TEK HÜCRELİ TIO₂ İNCE FİLM TABANLI
MEMRİSTİF CİHAZIN BÜYÜMESİ VE
KARAKTERİZASYONU

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ABSTRACT

In this thesis, we present the results of structural and electrical characterization for two types of experiments, producing single-cell memristor devices with different thicknesses. These devices are structured in the form of Si/SiO₂/Ta/Pt/TiO_x (5, 10, 15 nm)/Pt thin film stacks, and another thin film stack, Si/SiO₂/Ta/Pt/TiO_x (10 nm)/Pt, with square surface areas of 5 μm , 10 μm , 25 μm , and 50 μm on a maximum area of 10x10 mm² substrate, utilizing mask and optical lithography techniques.

Pt thin films were deposited for the upper and lower contacts of memristor devices using the magnetron sputter method. The metal oxide layer TiO₂ was grown in a Pulsed Laser Deposition (PLD) chamber under suitable growth conditions. The thickness of each layer in the device stack was measured using X-ray reflectivity (XRR), and the rates of composition and the structural properties of the metal oxide were identified using X-ray photoelectron spectroscopy (XPS) measurements. Subsequently, we examined the electrical characteristics, including memristive resistance switching of current–voltage curves, and the memristor devices exhibit synaptic functionalities, including spike-time-dependent plasticity (STDP), long-term potentiation (LTP), long-term depression (LTD), and endurance characteristics .

The results indicate that some of the fabricated devices exhibit suitability for non-volatile memory elements in CMOS technology, displaying digital switching performance, while others demonstrate analog memory characteristics. Additionally, we confirmed the multilevel conductance of the devices and observed that the thickness of the oxide layer can impact the resistive switching properties of the devices.

Keywords: Memristor, TiO₂, Memristive Behavior, Synaptic Plasticity.

ÖZET

Bu tezde, farklı kalınlıklara sahip iki tip deney için yapılan yapısal ve elektriksel karakterizasyonun sonuçlarını sunuyoruz. Bu cihazlar, Si/SiO₂/Ta/Pt/TiO_x (5, 10, 15 nm)/Pt ince film yığınları şeklinde yapılandırılmıştır. Ayrıca, başka bir ince film yığını olan Si/SiO₂/Ta/Pt/TiO_x (10 nm)/Pt, maksimum 10x10 mm² alt taban üzerinde 5 µm, 10 µm, 25 µm ve 50 µm kare yüzey alanlarına sahip olarak mask ve optik litografi tekniklerini kullanarak üretilmiştir.

Memristor cihazlarının üst ve alt temasları için Pt ince filmleri, magnetron sputter yöntemi kullanılarak biriktirilmiştir. Metal oksit tabakası TiO₂, uygun büyüme koşulları altında Pulsed Laser Deposition (PLD) odasında büyütülmüştür. Cihaz yığınındaki her tabakanın kalınlığı, X-ışını yansıma (XRR) kullanılarak ölçülmüş, metal oksidin bileşim oranları ve yapısal özellikleri ise X-ışını fotoelektron spektroskopisi (XPS) ölçümleri ile belirlenmiştir. Daha sonra, memristor cihazları için memristif direnç değişimi, spike-time-dependent plasticity (STDP), uzun süreli potansiyasyon (LTP), uzun süreli depresyon (LTD) gibi sinaptik fonksiyonlar ve dayanıklılık özellikleri de dahil olmak üzere elektriksel özellikleri inceledik.

Sonuçlar, üretilen bazı cihazların CMOS teknolojisinde kullanılmak üzere non-volatile bellek elemanları için uygun olduğunu göstermektedir; dijital anahtarlama performansını gösterirken, diğerleri analog bellek özellikleri sergilemektedir. Ayrıca, cihazların çok seviyeli iletkenlik gösterdiğini doğruladık ve oksit tabakasının kalınlığının cihazların direnç değiştirme özelliklerini etkileyebileceğini gözlemledik.

Anahtar Kelimeler: Memristör, TiO₂, memristif davranış, sinaptik plastisite.

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TABLE OF CONTENTS

	<u>Page</u>
ABSTRACT	vi
ÖZET	vii
ACKNOWLEDGEMENT	viii
TABLE of CONTENTS	x
LIST of ABBREVIATIONS and ACRONYMS	xi
LIST of FIGURES	xv
LIST of TABLES	xvi
1. INTRODUCTION	1
1.1. The Resistor	1
1.1.1. Ohm's law	1
1.2. The Capacitor	2
1.2.1. Current-voltage relation	4
1.3. The Inductor	5
1.3.1. Current-voltage relation	5
2. MEMRISTOR ORIGIN AND IT'S THEORETICAL DEFINITION	7
3. MEMRISTOR MODELS	9
3.1. HP Memristor Model	9
3.2. Nonlinear Drift Model and Window Function	11
3.2.1. Explanation of The Window Function	13
3.3. Simmons Tunneling Barrier Model	14
3.4. Threshold Adaptive Memristor Model (TEAM)	16
4. MEMRISTIVE SWITCHING	18
4.1. Thermal Switching	20
4.2. Electronic Switching	20
4.3. Switching Speed	21
5. MATERIALS FOR MEMRISTIVE DEVICE	22
5.1. TiO ₂ -Based Memristors	23
6. EXPERIMENTAL TECHNIQUES	25
6.1. Sample Preparation And Measurements Techniques	25
6.1.1. RF/DC Magnetron Sputtering	25
6.1.2. PLD Technique	26
6.1.3. XRD Technique	27
6.1.4. XRR Technique	29

6.1.5.	X-Ray Photoelectron Spectroscopy	30
6.1.6.	Lithography Technique	32
7.	EXPERIMENTS AND RESULTS	35
7.1.	Device Fabrication of Experiment 1	35
7.1.1.	Structural Characterization	37
7.1.1.1.	XRR	37
7.1.1.2.	XRD	39
7.1.1.3.	XPS	39
7.1.2.	Electrical Characterization	40
7.1.2.1.	I-V Curve Characterization	40
7.1.3.	Characterizing Synaptic Plasticity Performance	42
7.1.3.1.	Retention Measurement Results	44
7.1.3.2.	LTP and LTD Measurement Results	44
7.1.3.3.	STDP Measurement Results	45
7.2.	Device Fabrication Experiment 2	46
7.2.1.	Lithographic Processes of Fabricated Device	46
7.2.2.	Layers Growth Processes of Fabricated Device	48
7.2.3.	Structural Characterization of Experiment 2	50
7.2.4.	Electrical Characterization of Experiment 2	51
7.2.5.	AC Measurement For Synaptic Plasticity of Experiment2	53
7.2.5.1.	Retention Measurement Results	53
7.2.5.2.	LTP and LTD Measurement Results	54
8.	CONCLUSION	56
	REFERENCES	57
	BIOGRAPHY	62
	PUBLICATIONS WITHIN the SCOPE of THESIS STUDY	63

LIST of ABBREVIATIONS and ACRONYMS

$\text{\AA}$	: Angstrom
Φ	: Magnetic Flux
θ	: Angle
Hz	: Hertz
w	: Doped Thickness
eV	: Electron Volt
μ	: Average ion mobility
M	: Memristance
C	: Capacitance
I	: Current
L	: Inductance
λ	: Wavelength
f	: Frequency
v	: Velocity
E	: Electric Field
H	: Henries
J	: Current Density
Pa	: Pascal
F	: Farad
D	: Switch Thickness
V	: Voltage
νd	: Drift velocity
ρ	: Resistivity
LRS	: Low Resistance State
HRS	: High Resistance State
Q	: Charge
A(t)	: Amper
A	: Area
AC	: Alternative Current
CCD	: Current Controlled device
CPS	: Count Per Second
C	: Carbon
DC	: Direct Current
HP	: Hewlett-Packcard
HV	: High Vacuum
KrF	: Krypton difluoride
NI	: Nanotechnology Institute
nm	: Nanometer
O	: Oxygen
PLD	: Pulse laser deposition
Pt	: Platinum
SEM	: Scanning Electron Microscopy
Si	: Silicon
SiO ₂	: Silicon dioxide
Ta	: Tantalum
Ti	: Titanium

TiO ₂	:	Titanium Dioxide
TiO _{2-x}	:	Titanium Dioxide with Oxygen vacancy
UHV	:	Ultra High Vacuum
UV	:	Ultraviolet
VHV	:	Very High Vacuum
O	:	Oxygen
PLD	:	Pulse laser deposition
XPS	:	X-Ray Photoelectron spectroscopy
XRD	:	X-ray Diffraction
XRR	:	X-ray Reflection
I_p	:	Current Peak
W	:	Window Function
W	:	Tunnel Barrier
$f(V,m)$	:	Drift Function
I_{off}	:	Constant Parameter
I_{on}	:	Constant Parameter
I_{th}	:	Current Threshold
I_{off}	:	Current Threshold
TEAM	:	Threshold Adaptive Memristor
I_{off}	:	Constant Parameter for off State
I_{on}	:	Constant Parameter for on State
ReRAM	:	Resistive Random Access Memory
FR/D	:	Magnetron Sputtering
STDP	:	Short Term Depression Potentiation
LTP	:	Long Term Potentiation
LTD	:	Short Term Depression
RF	:	Radio Frequency
n	:	Integer
d	:	Interplanar Spacing
BE	:	Bottom Electrode
TE	:	Top Electrode
VDep	:	Voltage Depression
VPot	:	Voltage Potentiation
Δt	:	Relative Timing
Ar	:	Argon
R_s	:	Resistance Switching
Ω	:	ohms
MIM	:	metal insulator metal
V _O	:	oxygen vacancy

LIST OF FIGURES

	<u>Page</u>
Figure 1.1: Circuit symbol of a resistor. (left) US standard, and (right) IEC standard.	1
Figure 1.2: Current-voltage characteristics of a typical resistor	2
Figure 1.3: Circuit symbol of a capacitor.(left) Fixed capacitor, (center) polarized capacitor, (right)variable capacitor.	3
Figure 1.4: Voltage-current characteristics of a capacitor.	4
Figure 1.5: Circuit symbol of an inductor.	5
Figure 1.6: The current-voltage relation of an inductor.	6
Figure 2.1: The four equations that describe the fundamental attributes of two-terminal passive elements.	7
Figure 2.2: The current-voltage characteristic for the four basic elements in the case of a sinusoidal input voltage.	8
Figure 3.1: Schematic of HP memristor.	10
Figure 3.2: Memristor convention: a positive (negative) bias is determined by considering the applied voltage on the doped region as higher (lower) than that on the undoped region.	11
Figure 3.3: The memristor device model and circuit equivalent using Simmons tunneling current. The conductive channel is represented by a shunt resistor.	14
Figure 4.1: Typical current-voltage characteristics for (a) bipolar and (b) unipolar resistive switching (RS) .	19
Figure 4.2: Representation of filamentary conduction in MIM structures: (a) vertical stack, (b) lateral, planar configuration. The presence of the red tube signifies the filament responsible for the ON state (4).	20
Figure 5.1: Utilizing the periodic table, RRAM materials are selected for both the top and bottom electrodes, along with metal oxide (memristive) materials. Electrodes are represented in blue, while binary oxides are depicted in red, and (perovskite type) ternary oxides are presented in green.	22
Figure 5.2: Unit cell of a) rutile and b) anatase phase of TiO ₂ lattice structure. Red spheres represent oxygen and white spheres represent Ti atom.	23
Figure 6.1: Schematic of RF/DC magnetron sputtering.	26
Figure 6.2: Schematic of PLD.	27
Figure 6.3: Schematics of Bragg's law [19].	28
Figure 6.4: Schematic of the XRD mechanism.	28
Figure 6.5: Information of the x-ray reflectivity.	29
Figure 6.6: Schematic of XPS.	30
Figure 6.7: a) Occurring of the photoelectron, b) occurring of auger electron, c) emitting Fluorescence mechanism.	31
Figure 6.8: An example of XPS data TiO ₂ film on software.	32

Figure 6.9: Illustrates the arrangement for (a) top metal mask, (b) etch mask, and (c) bottom metal mask.	33
Figure 7.1: Nanotechnology Institute laboratory at Gebze Technical University.	35
Figure 7.2: Production process of the memristor device in Si/ SiO ₂ / Pt/ TiO _x (5, 10, 15) nm/Pt structure.	36
Figure 7.3: Single-cell memristor thin films prepared in Si/SiO ₂ /Ta/Pt/TiO _x /Pt stack structure.	37
Figure 7.4: Small angle X-ray reflection (XRR) results of the memristor device with SiO ₂ /Ta/Pt/TiO _x /Pt structure. Blue line show experimental data, and Red line shows simulation result. As a result of the simulation, the thickness, physical densities and roughness of each layer are shown in a table.	38
Figure 7.5: XRD result of SiO ₂ /Ta/Pt/TiO ₂ thin film.	39
Figure 7.6: Experimental and theoretical X-Ray Photo-electron spectroscopy (XPS) peaks of Ti and O in for samples with SiO ₂ /Ta/Pt/TiO _x /pt structure.	40
Figure 7.7: The current-voltage characteristics for TiO ₂ -based memristor devices with different thicknesses: a) 5 nm TiO _x device, b) 10 nm TiO _x device, c) 15 nm TiO _x device.	41
Figure 7.8: Endurance characteristics for TiO ₂ -based memristor devices with different thicknesses. a) Memristor device with 5 nm TiO ₂ thickness, b) 10 nm TiO ₂ thickness, c) 15 nm TiO ₂ thickness.	42
Figure 7.9: Potentiation and depression by applying AC pulse. Measured potentiating (1st pulse to 60th pulse) and depressing (61st pulse to 120th pulse) curves of the Si/SiO ₂ /Ta/pt/TiO _x /pt devices. a) Memristor device with 5 nm TiO ₂ thickness, b) 10 nm TiO ₂ thickness c) 15 nm TiO ₂ thickness.	43
Figure 7.10: Spike timing-dependent plasticity (STDP) with the structure of Si/SiO ₂ /Ta/pt/TiO _x /pt the relationship between the relative change of the memristor synaptic weight (Δw) and the relative spike timing (Δt). And the solid line is the exponential fitting curve to the experimental data. a) Memristor device with 5 nm TiO ₂ thickness, b) 10 nm TiO ₂ thickness c) 15 nm TiO ₂ thickness.	45
Figure 7.11: a) The mask design for the production of the bottom electrode layer (Blue), metal-oxide layer (Purple), and top electrode layer (Pink) for the memristor devices, b) The design includes single-cell memristor devices with different surface areas (5x5, 10x10, 25x25, and 50x50 μm^2), with 6 cells each, totaling 24 memristor cells in a 10x10 mm ² area, c) HEIDELBER–dwl666fs laser lithography system, d) Spin coating with positive photoresist, e) Heidelberg dwl666fs control panel and printing process, f) mask was exposed to light, g) Development process of the mask in AZ726 MIF chemical, h) Chrome mask ready for lithography after chrome etching.	47
Figure 7.12: Single-cell memristor thin films prepared in Si/ SiO ₂ / Ta/ Pt/ TiO _x (10)nm/Pt stack structure.	48
Figure 7.13: Bottom electrode lithography.	49

Figure 7.14: Device produced under room conditions in the PLD system.	50
Figure 7.15: a) XRD result of SiO ₂ /Ta/Pt/TiO ₂ thin film, b-c) High-resolution XPS spectra of Ti2p and O1s.	50
Figure 7.16: The current-voltage characteristics for TiO ₂ -based memristor devices with different surface areas in different cell contacts position and different voltage forming, a) Memristor device in the F contact cell with 50μ surface area without voltage forming for 50 cycles, b) memristor device in the F contact cell with 25μ surface area without voltage forming, c) memristor device in the F contact cell with 10μ surface area without voltage forming, d) memristor device in the E contact cell with 25μ surface area with forming of (1.5V, 1sec), e) memristor device in the E contact cell with 5μ surface area with forming of (-1V, 1sec), f) memristor device in the D contact cell with 25μ surface area with forming of (-2V, 1sec).	51
Figure 7.17: The current-voltage characteristics for TiO ₂ -based memristor devices, a) memristor device in the F contact cell with 5μ surface area without voltage forming, b) memristor device in the E contact cell with 10μ surface area with forming of (1.5V, 1sec), c) memristor device in the E contact cell with 5μ surface area with forming of (1V, 1sec), d) memristor device in the D contact cell with 10μ surface area with forming of (2V, 1sec), e) memristor device in the D contact cell with 10μ surface area with forming of (-1.5, 500ms).	52
Figure 7.18: The current-voltage characteristics for TiO ₂ -based memristor devices with low ROFF/RON ratio, a) memristor device in the D contact cell of 50μ surface area with voltage forming (2V, 1sec), b) memristor device in the D contact cell of 50μ surface area with forming of (-2V, 1sec), c) memristor device in the D contact cell of 25μ surface area with forming of (-2V, 1sec).	53
Figure 7.19: Retention characteristics of the memristor devices with different surface areas, a) Memristor device of 5μ Surface area, b) Memristor device of 10μ Surface area, c) Memristor device of 25μ Surface area, d) Memristor device of 50μ Surface area.	54
Figure 7.20: Potential (60 pulses) and Depression (60 pulses) by applying 120 consecutive pulses in SiO ₂ /Ta/Pt/TiO ₂ /Pt devices. Gradual current change of memristor devices a) Memristor device with 5 x 5 μ surface area, b) Memristor device with 10 x10 μ surface area, c) Memristor device with 15 x15 μ surface area.	55

LIST OF TABLES

	<u>Page</u>
Table 3.1: Comparison of different memristor models.	17
Table 7.1: XPS fitting parameters of SiO ₂ /Pt/TiO _x (13.5nm).	38

1. INTRODUCTION

Before delving into the concept of the memristor as the element that has been absent, it is worthwhile to provide an overview of the conventional circuit components, including the resistor, capacitor, and inductor, purely for the purpose of drawing comparisons [1].

1.1. The Resistor

A resistor is a two-terminal, linear, passive fundamental circuit element that is designed to restrict the flow of electric current in a circuit. It is characterized by its electrical resistance, which is measured in ohms (Ω). Resistor devices are typically made of materials with properties that impede the movement of electrons, such as carbon, metal alloys, or semiconductors. Figure 1.1 shows the symbols for the resistor.

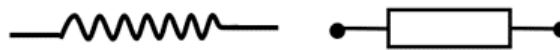


Figure 1.1: Circuit symbol of a resistor. (left) US standard, and (right) IEC standard.

The primary function of a resistor is to regulate the amount of current passing through a circuit by converting electrical energy into heat energy. This is achieved through the process of resistance, which opposes the flow of electrons and leads to a voltage drop across the resistor.

Resistors are used for various purposes in electronic circuits, including limiting current to protect components, dividing voltage in voltage dividers, adjusting signal levels, and controlling the time constants in RC circuits. They come in various shapes, sizes, and resistance values to suit different applications and are an essential component in the design and operation of electronic devices and systems.

1.1.1. Ohm's law

In accordance with Ohm's law, the voltage across a resistor is directly related to the current passing through it and this relationship is determined by a constant factor known

as resistance. In simpler terms, Ohm's law establishes that current is directly linked to voltage and inversely related to resistance.

$$V = IR \quad (1.1)$$

Equivalently, Ohm's law can also be written as:

$$R = V/I \quad (1.2)$$

Consequently, when resistance is higher, the current flowing through a circuit is reduced. In Figure 1.2 below, you can observe the voltage-current relationship for resistor.

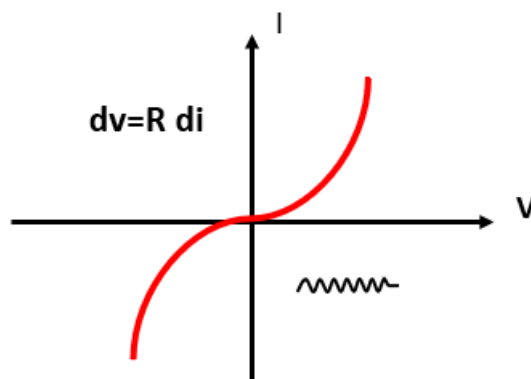


Figure 1.2: Current-voltage characteristics of a typical resistor

1.2. The Capacitor

A capacitor is a passive electronic component with two terminals. It comprises two conductive plates separated by a non-conductive dielectric material. Its primary function is to store electric charge. When a voltage difference is applied across the capacitor's conductive plates, dipole ions within the dielectric become polarized. The polarization induces the accumulation of positive ions on one capacitor plate and negative ions on the opposing plate, leading to the establishment of equal and opposite charges on the facing surfaces of the plates. This configuration creates a static electric field within the dielectric, facilitating the storage of electric charge in the medium. The dielectric material serves two important purposes: first, it reduces the strength of the electric field

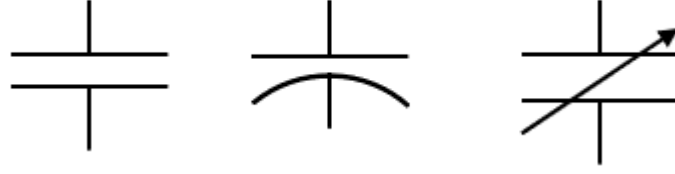


Figure 1.3: Circuit symbol of a capacitor.(left) Fixed capacitor, (center) polarized capacitor, (right)variable capacitor.

between the plates, increasing the capacitor's capacitance (its ability to store charge); second, it provides insulation that prevents excessive current leakage between the plates and limits the electric field strength, preventing a breakdown in voltage. The circuit symbol is shown in Figure 1.3.

Capacitors find widespread use in numerous applications, serving functions such as charge storage, DC blocking while permitting AC passage, smoothing power supply circuit outputs, coupling between two circuit stages, constructing filter networks, enabling delay functions, and tuning radios to specific frequencies. Capacitors come in various types, including fixed and variable, and they can be further categorized as polarized or non-polarized. Electrolytic capacitors exemplify polarized capacitors, whereas the majority of capacitors with lower values are non-polarized. An ideal capacitor's key characteristic is its capacitance, measured in Farads (F). It's defined, as depicted in equation (1.3), as the proportion of electric charge accumulated on individual conductor plates to the voltage difference between them. To provide a practical sense, one Farad represents the capacitance When a capacitor stores one coulomb of charge through the application of one volt across it.

$$C = Q/V. \quad (1.3)$$

In which Q represents the quantity of charge stored within the capacitor, C denotes the specific capacitance value, and V signifies the applied voltage across the capacitor. If there happens to be a alteration in the capacitance, it can be expressed in terms of incremental adjustments.

$$C = \frac{dq}{dv}. \quad (1.4)$$

The current passing through a capacitor is given by:

$$I = C \frac{dv}{dt}. \quad (1.5)$$

1.2.1. Current-voltage relation

As per the definition, the current flowing through the capacitor signifies the pace at which charge is moving through it. The presence of the dielectric material prevents charges and electrons from traversing the insulating layer; instead, they gather on the negative plate. For each electron that departs from the positive plate, a hole with an equal but opposite charge (a positive charge) emerges on the opposite plate. Consequently, the charge on the electrodes equals the integral of the current and is likewise proportionate to the voltage. This leads to the capacitor equation, which can be expressed in integral form as:

$$v(t) = \frac{q(t)}{C} = \frac{1}{C} \int_{t_0}^t i(\tau) d\tau + v(t_0) \quad (1.6)$$

The derivative form can be derived by differentiating the equation provided above.

$$i(t) = \frac{dq(t)}{dt} = C \frac{dv(t)}{dt}. \quad (1.7)$$

the relationship between current and voltage in a capacitor is shown in Figure 1.4.

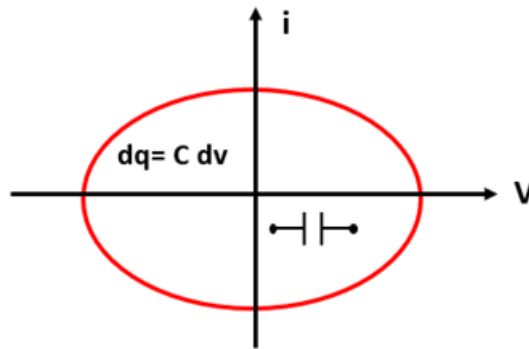


Figure 1.4: Voltage-current characteristics of a capacitor.

1.3. The Inductor

An inductor is a passive component with two terminals that stores energy within a magnetic field. This concept was initially introduced by Michael Faraday in 1831. The defining attribute of an inductor is its inductance, which is quantified in units of Henries (H). While nearly any conductor possesses inductance, it is common practice to coil or loop them to enhance the strength of the magnetic field. The circuit symbol is shown in Figure 1.5.



Figure 1.5: Circuit symbol of an inductor.

Faraday's law of electromagnetic induction stipulates that a voltage is generated when there is a changing magnetic field inside a coil over time. In accordance with Lenz's law, this induced voltage acts in opposition to the change that initially caused it. Due to their capability to delay or reshape alternating currents, inductors find extensive application in electronics, especially in situations where voltage and current exhibit time variations. Inductors can vary in types, primarily based on the core they employ, including air core inductors, ferromagnetic core inductors, and variable inductors. A specific category of inductors known as chokes is utilized in power supply filters or to block AC signals.

1.3.1. Current-voltage relation

Within an electrical circuit, an inductor counteracts alterations in the current flowing through it by generating a voltage that corresponds to the rate of change in that current. While the concept of an ideal inductor implies no resistance, in practical terms, only superconducting inductors exhibit actual zero resistance. The connection between voltage, denoted as $v(t)$, and current, represented as $i(t)$, in an inductor can be described by the following differential equation:

$$v(t) = L \frac{di(t)}{dt}, \quad (1.8)$$

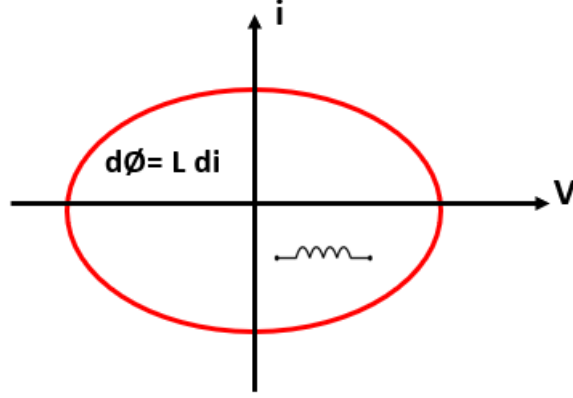


Figure 1.6: The current-voltage relation of an inductor.

where L signifies the inductance. When an inductor experiences a sinusoidal alternating current, it will produce a sinusoidal voltage in response.

$$i(t) = I_{\rho} \sin (2\pi ft), \quad (1.9)$$

where I_{ρ} represents the current's peak amplitude, and f denotes the current's frequency. The amplitude of the voltage is directly linked to the product of the current's frequency and its amplitude, as

$$v(t) = L \frac{di(t)}{dt}, \quad (1.10)$$

where

$$\frac{di(t)}{dt} = 2\pi f I_{\rho} \cos(2\pi ft). \quad (1.11)$$

When an inductor is linked to a current source in conjunction with a resistor, the current source essentially creates a short circuit, causing the current to diminish in an exponential decay pattern:

$$i(t) = I e^{\frac{R}{L}t}. \quad (1.12)$$

The current-voltage relation of an inductor is shown in Figure 1.6.

2. MEMRISTOR ORIGIN AND IT'S THEORETICAL DEFINITION

The inception involves a theoretical delineation of the memristor device [2–4]. Serving as a fundamental circuit component, the memristor is characterized by a distinctive relationship among electrical parameters. Each of the two passive terminal elements is explicated by establishing a connection between two of the four fundamental electrical quantities: electrical flux (Φ), charge (Q), current (I), and voltage (V), as depicted in Figure 2.1.

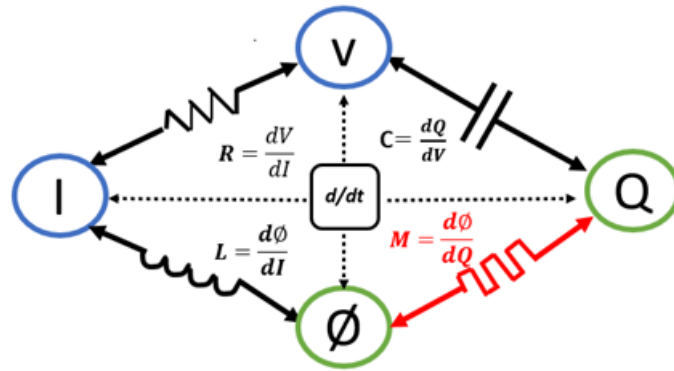


Figure 2.1: The four equations that describe the fundamental attributes of two-terminal passive elements.

The unexplored correlation between charge and flux was the critical factor leading Dr. Leon Chua to propose the existence of memristor devices in the 1970s. Thus, this would bring the cycle full circle, where the resistor establishes the connection between current and voltage, the inductor governs the relationship between current and flux, and the capacitor manages the association between voltage and charge. In contrast to the other primary passive devices, the memristor stands out as the sole device exhibiting a current hysteresis response to a periodic voltage input. This distinctive response cannot be replicated through any conceivable combination of the other two-terminal passive devices. Figure 2.2 depicts the I-V relation for the four core devices when subjected to a periodic voltage waveform input. The resistor is characterized by a linear or nonlinear relationship between voltage and current, akin to that of a diode. Capacitors and induc-

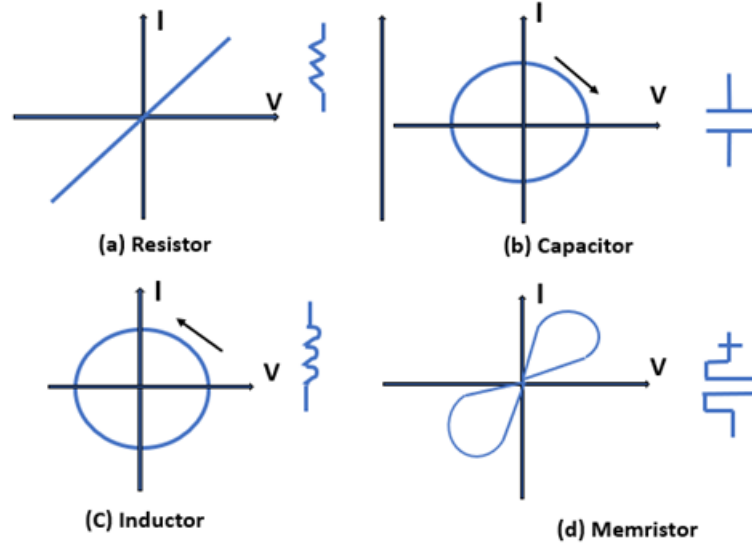


Figure 2.2: The current-voltage characteristic for the four basic elements in the case of a sinusoidal input voltage.

tors serve as energy-storing elements, maintaining a $\pm 90^\circ$ phase difference. Conversely, memristors introduce a variable phase difference between voltage and current.

This occurs because the device's resistance, governing the relationship between voltage and current, undergoes changes. Nevertheless, the device does not store any energy, and at zero voltage, no current flows through it. This indicates that the envisioned memristor has the capacity to retain a resistance value even after disconnecting the power source from the device. Unlike capacitors and inductors, it doesn't function as an energy storage device, requiring the voltage to be zero when the current reaches zero. Consequently, the I-V curve of the device forms a pinched hysteresis loop, underscoring the presence of a memory effect.

A few years later, Dr. Chua and Dr. Sung Mo Kang conducted additional research on the theoretical memristor device, categorizing the memristor as a subset of a broader class known as memristive systems [3]. Similar to memristors, all memristive systems must exhibit zero output when the input is zero, setting them apart from arbitrary dynamical systems. Until the successful fabrication of a memristor device was first reported in 2008 [5], the memristor had been regarded merely as a mathematical curiosity.

3. MEMRISTOR MODELS

Memristors find applications in a wide array of fields, each demanding specific characteristics. Take logic and memory applications, for instance; they require elements capable of performing computations, exerting control, and storing data efficiently post-computation. These applications necessitate swift read and write operations, with a reading mechanism that doesn't alter the data during retrieval. Other key considerations for memristor applications encompass scalability, low power consumption, and compatibility with traditional CMOS technology and for this numerous circuit models for the memristor have been introduced in the literature [5–15]. These models range from purely theoretical to highly accurate physical representations. In this section, we delve into the four primary approaches for modeling the memristor device, as outlined in the literature.

3.1. HP Memristor Model

The initial creation of a memristor device occurred under the guidance of Dr. Stanley Williams by a research team at HP Labs [5]. This team was established in 1995 with the primary objective of enhancing computing power as transistors approached their minimum size limit. Their solution involved the development of a nanoscale crossbar array of switches designed to ensure system functionality even in the presence of defective components [16]. The HP memristor device comprises a two-terminal structure featuring a Si/SiO₂/Pt/TiO_{2-x}/TiO₂/Pt stack thin-film architecture positioned between two Pt electrodes. Within the active oxide region, a segment of TiO_{2-x} with oxygen vacancies coexists with another segment of pure TiO₂ thin film. While oxygen vacancies (Vo) contributions are dispersed throughout the device, their concentration at one end is negligible in comparison to the Vo concentration in the opposite end region. This ratio effectively divides the device into two regions, each characterized by distinct resistances. The device's behavior is contingent upon the polarity of the applied voltage or the direction of current flow, causing the boundary between doped and undoped regions to shift forwards or backwards within the device. According to the model depicted in Figure 3.1, as the boundary shifts leftward, the thickness (w) of the

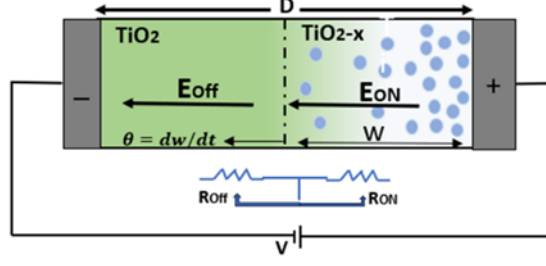


Figure 3.1: Schematic of HP memristor.

low-resistance region ($\text{TiO}_2\text{-x}$ with higher oxygen vacancy density) increases, while the thickness ($D-w$) of the high-resistance region (TiO_2 with lower oxygen vacancy density) decreases, resulting in a transition to a low-resistance state (LRS). Conversely, altering the voltage polarity prompts the boundary to move rightward, augmenting the thickness of the high-resistance region (TiO_2) and diminishing the thickness of the low-resistance region ($\text{TiO}_2\text{-x}$), leading to a shift to a high-resistance state (HRS). These behaviors, contingent on voltage polarity, validate the device's characteristic of exhibiting a bipolar resistance switching feature. When the current flow to the device ceases, the movement of the boundary between the low-resistance (LR) and high-resistance (HR) regions suspend. Upon reapplication of current, the boundary resumes movement from where it left off, even after extended periods, making 'w' the state variable that signifies the instantaneous memristance of the device.

When a positive voltage is applied to the device, current starts to flow and the voltage takes on two different values, V_1 and V_2 , in the doped and undoped regions respectively.

$$V_1 = R_{\text{on}} \frac{w}{D} i(t) = R_{\text{on}} \frac{w}{D} \frac{v(t)}{R_{\text{on}} \frac{w}{D} + R_{\text{off}} (1 - \frac{w}{D})}, \quad (3.1)$$

$$V_2 = R_{\text{off}} (1 - \frac{w}{D}) i(t) = R_{\text{off}} (1 - \frac{w(t)}{D}) \frac{v(t)}{R_{\text{on}} \frac{w}{D} + R_{\text{off}} (1 - \frac{w}{D})}. \quad (3.2)$$

The device was determined to be functioning by the migration of the charged vacancies in the oxygen deficient layer. Basic HP memristor equation state has been shown as Equation(3.3) and Fig 3.2 at any time , where D is the total length of the device and w is the state variable [17].

$$M(t) = \left(R_{\text{on}} \frac{w(t)}{D} + R_{\text{off}} \left(1 - \frac{w(t)}{D} \right) \right). \quad (3.3)$$

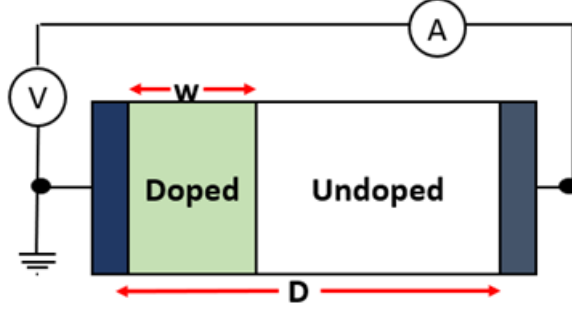


Figure 3.2: Memristor convention: a positive (negative) bias is determined by considering the applied voltage on the doped region as higher (lower) than that on the undoped region.

HP Labs has subsequently released numerous additional research papers centered around the characterization of the TiO₂ memristors they developed [18–26] and has garnered significant attention due to its potential applications in various areas of electronics. Its unique characteristics make it suitable for high-density memory storage, offering advantages in terms of speed, energy efficiency, and scalability compared to traditional memory technologies. Additionally, the memristor’s ability to emulate synaptic behavior has positioned it as a key player in neuromorphic computing, where it can potentially revolutionize artificial intelligence applications by mimicking the learning and memory processes observed in biological systems. In summary, the HP memristor model represents a significant advancement in electronic devices, providing a promising avenue for the development of efficient and versatile memory technologies with applications ranging from high-density data storage to neuromorphic computing.

3.2. Nonlinear Drift Model and Window Function

Due to the nanoscale dimensions of memristor devices, applying low voltages to these devices generates strong electric fields and triggers non-linear ionic conduction within the device. Specifically, in oxide materials where oxygen vacancies can only move between two metal electrodes (without penetrating the metal electrodes), non-linear effects impacting ionic conduction are most pronounced at the device edges, denoted as points with $w=0$ and $w=D$. This is because as vacancy defects approach these boundaries, their drift velocities decrease substantially, nearing zero. The drift velocity relies

on both the mobility of charge carriers and electric fields, influencing the dynamics of the device's state variables, current, and, consequently, overall behavior. Notably, the HP linear drift model overlooks these highly significant non-linear effects occurring at the device edges. In accordance with the linear drift model, the position of the boundary separating areas with and without oxygen vacancies (Vo) within the device as shown in Figure 3.1, the TiO₂-x/TiO₂ boundary and the tunnel barrier width (w) are directly linked to charge, as indicated by the following equation:

$$w(t) = w_0 + \mu \frac{R_{\text{on}}}{D} (q(t) - q_0). \quad (3.4)$$

However, this linear relationship loses its physical significance when approaching the device's edges (where $w=0$). In practical terms, conduction relies on positively charged vacancy defects, and the condition $w=0$ never occurs, as this would imply the absence of defect carriers essential for conduction within the device. Therefore, a more precise representation of the linear drift model is required. From a physical standpoint, the drift velocities of charge carriers should reach a maximum at the center of the device and gradually decrease as they approach the boundaries, analogous to the behavior seen in the mass-spring problem. To account for the boundary effects, we can introduce a "dimensionless window function" into the equation governing state variable dynamics, which is contingent on w [27],

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{\text{on}}}{D} \cdot i(t) \cdot f\left(\frac{w}{D}\right). \quad (3.5)$$

The function f in this context is a dimensionless function that represents the contribution of nonlinear effects at the device boundaries. The initial window function was proposed by Strukov [5] as follows

$$f\left(\frac{w}{D}\right) = \frac{w(D-w)}{D^2} = \left(\frac{w}{D}\right) - \left(\frac{w}{D}\right)^2, \quad (3.6)$$

and with its normalized form

$$f(x) = x(1-x), \quad \text{for } x = \frac{w}{D}. \quad (3.7)$$

The window function ensures that the drift velocity is zero when $w = 0$ and D . On the other hand, it is compatible with the linear drift model as we move away from the boundary regions. It only allows nonlinear effects to dominate near the boundary regions i.e., memristors often exhibit strong nonlinearity at their boundaries, where the

memristance transitions between different states. This nonlinear behavior can significantly impact the memristance change, and the window function helps capture these effects.

3.2.1. Explanation of The Window Function

1. *Window function as deviation:* The window function, $w(V,M)$, where V could represent a variable or parameter that influences the shape or characteristics of the window function and M could represent another variable or parameter that influences the behavior of the window function. This window function quantifies the deviation or the difference between the actual rate of change in memristance (dt/dM) and what the drift function predicts $f(V,M)$. In other words, it measures how far the memristance's behavior diverges from the idealized model.
2. *Nonlinear effects at boundaries:* Memristors often exhibit strong nonlinearity at their boundaries, where the memristance transitions between different states. This nonlinear behavior can significantly impact the memristance change, and the window function helps capture these effects.
3. *Utility in modeling:* The window function is a valuable tool for modeling and simulating memristor behavior accurately. By considering the deviations between actual and predicted memristance changes, it enables a more realistic representation of memristor dynamics in various applications, such as memory devices and neuromorphic computing.

In summary, the window function in memristors serves as a crucial element in understanding and modeling the nonlinear behavior of these devices. It helps bridge the gap between theoretical predictions (drift function) and actual device behavior, allowing for a more accurate representation of memristor dynamics, particularly in scenarios where nonlinearity is prominent, such as at device boundaries.

To sum up, In this model the migration of oxygen vacancies within the memristor's insulating layer is a central concept. When a voltage is applied, these vacancies drift through the insulator, creating or disrupting conductive paths. The movement of oxygen vacancies is inherently nonlinear, and it becomes increasingly challenging for them to travel as the conductive paths grow longer. This nonlinearity arises from factors such

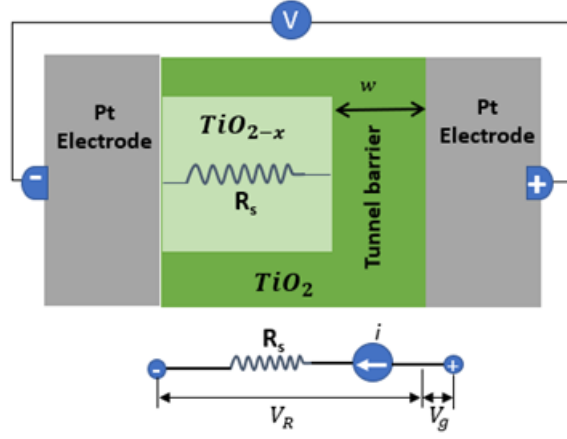


Figure 3.3: The memristor device model and circuit equivalent using Simmons tunneling current. The conductive channel is represented by a shunt resistor.

as the decreasing concentration of vacancies and the increasing energy barrier encountered as the migration distance extends. The Nonlinear Drift Model accounts for the non-volatile nature of memristor behavior, meaning the altered resistance state persists even after the removal of the applied voltage. Reversibility is also a crucial aspect of this model, as applying a voltage of opposite polarity can annihilate the conductive filaments, returning the memristor to its initial resistance state and understanding this Model is essential for optimizing memristor design and performance. Researchers leverage this model to explore strategies for enhancing switching speed, endurance, and reliability.

3.3. Simmons Tunneling Barrier Model

The earlier models were founded on HP's physical depiction of memristors, which involved two doped and undoped oxide regions, each represented as a resistor. However, Pickett and colleagues presented a more precise physical model of memristors in their work [20]. In this new model, instead of two resistors in a series, as seen in HP's model, a resistor is connected in series with an electron tunnel barrier shown in Figure 3.3.

This model demonstrates switching characteristics that are both nonlinear and asymmetric. The width of the Simmons tunnel barrier [28] is considered the state variable, denoted as " w ". Consequently, differentiating " w " corresponds to the oxygen vacancy drift velocity. Applying a positive voltage or current to the top electrode increases

the tunnel barrier width (and thus the state variable), leading to an exponential rise in device resistance. Conversely, applying a negative voltage decreases the width, resulting in an exponential decline in device resistance. This bipolar behavior, explained by the tunneling current, is also in line with modeling involving mobile dopant ions, oxygen vacancies, and electrochemical reactions within the insulating barrier. Simmons, in 1971, computed the current value for thin films within a Metal/Metal-oxide/Metal structure. This particular current, distinct from the ionic current occurring in TiO₂, is denoted as the “Ohmic electronic current”,

$$i = \frac{J_o A}{\Delta w^2} \left\{ \phi e^{-B\sqrt{\phi}} - (\phi + e|V_g|) e^{-B\sqrt{(\phi + e|V_g|)}} \right\}, \quad (3.8)$$

where

$$\phi = \phi_o - e|V_g| \frac{w_1 + w_2}{w} + \frac{1.15\lambda w}{\Delta w} \ln \left(\frac{w_2(w - w_1)}{w_1(w - w_2)} \right), \quad (3.9)$$

and

$$w_1 = 1.2\lambda w / \phi_o \text{ and } w_2 = w_1 + w \left(1 - \frac{9.2\lambda}{3\phi_o + 4\lambda - 2e|V_g|} \right), \quad (3.10)$$

and

$$B = 4\pi\Delta w\sqrt{2m}/h \text{ and } L = e^2 \ln(2) / (8\pi k\epsilon_o). \quad (3.11)$$

Here Conductive channel’s average cross-sectional area A , e electronic charge, h Planck constant, Δw insulating barrier width, ϕ_o insulating barrier height, $k=5$, dielectric constant, ϵ_o vacuum permittivity, $\lambda = L/w$, w_1 , and w_2 positions of the barrier potentials relative to the Fermi level. The tunnel barrier width is considered as a state variable and to elucidate the experimentally observed asymmetric hysteresis behavior, the dynamic equation for the state variable is provided as a function of the polarity of the applied voltage (or the direction of the applied current) as follows:

$$\frac{dw}{dt} = \begin{cases} f_{\text{off}} \sinh \left(\frac{i}{i_{\text{off}}} \right) \exp \left[-\exp \left(\frac{w - a_{\text{off}}}{w_c} - \frac{[i]}{b} \right) - \frac{w}{w_c} \right], & i > 0 \text{ (off switching)} \\ f_{\text{on}} \sinh \left(\frac{i}{i_{\text{on}}} \right) \exp \left[-\exp \left(\frac{w - a_{\text{on}}}{w_c} - \frac{[i]}{b} \right) - \frac{w}{w_c} \right], & i < 0 \text{ (on switching)} \end{cases}, \quad (3.12)$$

where f_{off} , f_{on} , a_{off} , a_{on} , i_{off} , i_{on} , and b represent the parameters used for fitting. f_{on} is notably larger in magnitude compared to f_{off} , and both of these parameters influence the magnitude of the w change. i_{on} and i_{off} effectively determine the current threshold, which is valuable in digital applications. Specifically, a_{off} sets the upper limit, while a_{on}

establishes the lower limit for w . In this model, the transition rate from a high-resistance state to a low-resistance state (on-switching) is significantly faster than off-switching. It has been asserted that the Simmons tunnel barrier model is currently considered the most precise physical representation of memristors. However, this model has encountered some challenges:

- It is difficult.
- The correlation between current and voltage is not explicitly specified.
- Its applicability is limited in scope, as it is tailored to a specific type of memristor and does not encompass all memristor variations.

3.4. Threshold Adaptive Memristor Model (TEAM)

The TEAM model, as introduced by Kvatinsky et al. [11], offers a straightforward and versatile approach. It essentially encapsulates the same underlying physical model (the Simmons tunnel barrier model), but with notably simpler mathematical expressions. To streamline analysis and computational efficiency, a few assumptions are made:

1. Below a specific threshold, the state variable remains constant.
2. Instead of relying on exponential relationships, the model employs polynomial relationships to describe the connection between memristor current and the derivative of the internal state drift.

This TEAM model can be adapted to fit various memristor models, including the Simmons tunnel barrier model. The relationship between the derivative of the internal state and both current and the state variable can be represented by the multiplication of two independent functions: one associated with current and the other dependent on the state variable “ w ”. Therefore, the derivative of the state variable will be:

$$\frac{dw(t)}{dt} = \begin{cases} K_{\text{off}} \left(\frac{i(t)}{i_{\text{off}}} - 1 \right)^{a_{\text{off}}} \cdot f_{\text{off}}(w), & 0 < i_{\text{off}} < i \\ 0, & i_{\text{on}} < i < i_{\text{off}} \\ K_{\text{on}} \left(\frac{i(t)}{i_{\text{on}}} - 1 \right)^{a_{\text{on}}} \cdot f_{\text{on}}(w), & i < i_{\text{on}} < 0 \end{cases} \quad (3.13)$$

Here, we have constants represented as K_{off} , K_{on} , a_{off} , and a_{on} , with the conditions that K_{off} is greater than 0 and K_{on} is less than 0. We also have current thresholds i_{off} and i_{on} , along with the internal state variable w . The functions $f_{\text{off}}(w)$ and $f_{\text{on}}(w)$ serve as

window functions, effectively restricting the range of w to fall within the boundaries defined by $[w_{\text{off}}, w_{\text{on}}]$. It's worth noting that these two functions don't necessarily have to be identical, resembling the asymmetric dependency on w found in the Simmons tunnel barrier model. The comparison of different memristor models are shown in Table 3.1 [11].

Table 3.1: Comparison of different memristor models.

Model	Linear ion drift	Non-linear ion drift	Simmons tunneling barrier	TEAM
State variable	$0 \leq w \leq D$ Doped region physical width	$0 \leq w \leq D$ Doped region normalized width	$a_{\text{off}} \leq x \leq a_{\text{on}}$ Undoped region width	$a_{\text{on}} \leq x \leq a_{\text{off}}$ Undoped region width
Control mechanism	Current-controlled	Voltage-controlled	Current-controlled	Current-controlled
Current-voltage relationship and memristance deduction	Explicit	I-V relationship: explicit memristance deduction ambiguous	Ambiguous	Explicit
Matching memristive system definition	Yes	No	No	Yes
Generic	No	No	No	Yes
Accuracy comparing practical memristors	Lowest accuracy	Low accuracy	Highest accuracy	Sufficient accuracy
Threshold exists	No	No	Practically exists	Yes

4. MEMRISTIVE SWITCHING

Memristive switching refers to the ability of a memristor to switch between two distinct resistance states, often referred to as the “off” and “on” states. These states can be thought of as high and low resistance values. Therefore, by applying voltage or current to a memristor, significant changes in resistance can occur, rendering memristors suitable for use as switches. Numerous metal-insulator-metal (MIM) systems exhibit resistive switching effects, laying the groundwork for the development of emerging non-volatile memory technologies. The insulator component within the MIM structure can encompass various binary or multinary oxides, chalcogenides, and organic compounds. Likewise, the selection of metals for electrodes and electron-conductive non-metals offers a broad range of possibilities.

According to the findings of Waser and Aono [29], resistive memories employ two distinct switching mechanisms:

- *Cation migration*: This relies on the electrochemical growth and dissolution of metallic filaments.
- *Anion migration*: In this method, sub-oxide conductive pathways are established and suppressed through localized redox processes. More extensive explanations of these mechanisms can be found in Waser and Aono’s work [29].

As delineated in the same source [29], the type of resistive switching in MIM systems depends on the electrical polarity required:

- *Unipolar*: In unipolar switching, the switching process occurs irrespective of the polarity of voltage and current, allowing for switching regardless of the direction of these parameters.
- *Bipolar*: Conversely, bipolar switching hinges on the voltage and current polarity. In this case, the ON and OFF switching events occur under different polarities, necessitating a specific direction for effective switching.

In both unipolar and bipolar switching mechanisms, it is crucial to perform state reading at a low voltage to ensure that the state remains modified during the reading process. The system transitions, or “sets”, from the OFF state (characterized by high resistance)

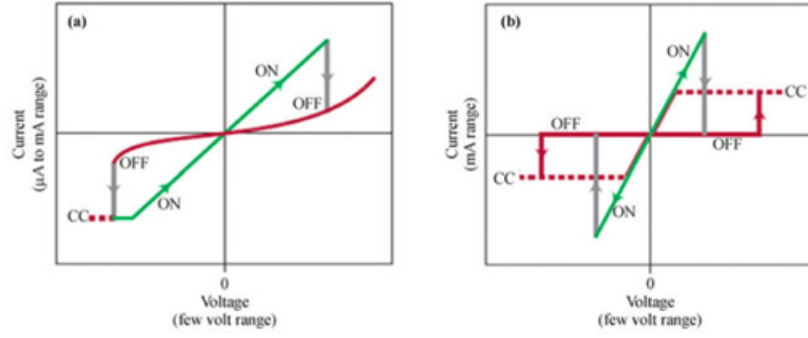


Figure 4.1: Typical current-voltage characteristics for (a) bipolar and (b) unipolar resistive switching (RS) .

to the ON state (with low resistance) by applying a threshold voltage. The control circuit's compliance current, denoted as "CC", serves as a limiting factor for the current. Reverting to the OFF state, or "resetting", occurs at a significantly higher current level than the switching current, and it requires a threshold voltage smaller than the ON threshold voltage, which is not necessarily negative. As previously mentioned, bipolar switching is identified by the ON state occurring at a specific threshold voltage and the OFF state also occurring at the same threshold voltage but with reversed polarity. To demonstrate bipolar behavior, the structure must exhibit some form of imbalance, which could be attributed to varying electrode materials or differing voltage polarities in the initial stages. Figure 4.1 provides examples of unipolar and bipolar curves [30].

Now, let's delve into the precise location within the oxide where the switching mechanism takes place and the factors driving it. It has been documented that instead of spreading uniformly across the entire pad or contact area, the transition to the ON state is confined to a filament [29]. This results in a resistance level that remains consistent irrespective of the pad's size. Figure 4.2 illustrates both vertical and lateral configurations of the metal-insulator-metal (MIM) sandwich structure, showcasing the filament-based nature of the switching mechanism [31]. The red filament is the element responsible for driving the state change. The underlying mechanisms governing the switching process involve a combination of physical and/or chemical effects, which can be categorized into three classifications: thermal, electronic, or ionic [29].

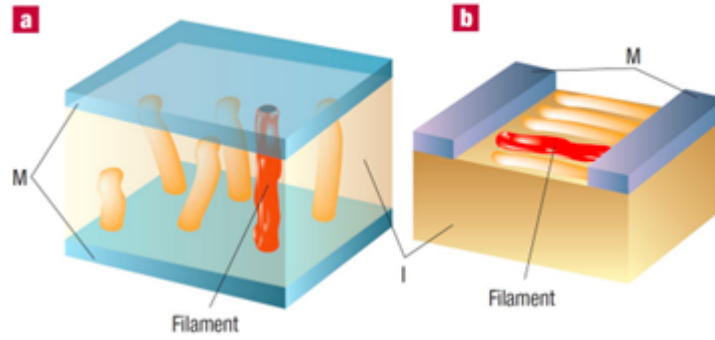


Figure 4.2: Representation of filamentary conduction in MIM structures: (a) vertical stack, (b) lateral, planar configuration. The presence of the red tube signifies the filament responsible for the ON state (4).

4.1. Thermal Switching

In the case of thermal switching, changes in the material occur through Joule heating, leading to modifications in a discharge filament, often referred to as partial dielectric voltage breakdown. This type of switching is unipolar in nature. Controlled resistance is achieved through the presence of a compliance current, resulting in the formation of a relatively weak conductive filament. This particular switching mechanism is sometimes termed the “fuse-antifuse” mechanism. During the reset process, the filament is disrupted due to the exceptionally high power density, around 10^{12} W/cm³. Titanium dioxide can exhibit bipolar switching characteristics, but if the compliance current is sufficiently high and no breakdown occurs, it can demonstrate unipolar switching behavior.

4.2. Electronic Switching

In this mechanism, due to the nano-scale dimensions of the Metal/Metal-Oxide/Metal memristor device, it is known that initially applying a certain voltage for a certain period of time (electroforming) causes the formation of oxygen vacancy defects, local heating, and irreversibly reduces the resistance of the region from giga-ohm levels to kilo-ohm (on/off switching levels) levels within the insulating metal oxide layer. Additionally, this process creates a conductive channel with a resistance of a few hundred ohms within the metal oxide layer, which serves as a shunt resistance. The applied voltage

changes the distance between the conductive channel and the other metal electrode, allowing for electron tunneling current to occur through the quantum tunneling effect.

4.3. Switching Speed

In practice, the process of switching to the ON state in a memristor occurs significantly faster than switching back to the OFF state. This speed difference arises from distinct mechanisms governing drift and diffusion currents. The drift current is a result of oxygen vacancies moving due to the internal electric potential, while the diffusion current involves the migration of oxygen vacancies from TiO_{2-x} to TiO_2 . When a positive voltage is applied to the device, these two currents act in opposing directions. However, when a negative voltage is applied, both the drift and diffusion currents align in the same direction [32, 33].

5. MATERIALS FOR MEMRISTIVE DEVICE

A typical memristor or resistive memory exhibits a metal-insulator-metal (MIM) configuration, where metals serve as the upper and lower contacts, and the insulator typically consists of a resistive switching material, often transition metal oxides. The properties of materials play a crucial role in determining the performance of nanoscale devices. Various materials can be employed, leading to diverse characteristics and capabilities. Memristive devices, including resistive random access memories (ReRAM), utilize a wide range of materials.

The periodic table is color-coded to show materials used in memristive devices. The legend indicates:

- Blue:** Electrode materials (Pt, TiN/Ti, TiN, Ru, Ni, Ag, Au, Pd, Ir, Cu, ...)
- Red:** Electrode materials (TiO_x, NiO_x, HfO_x, WO_x, TaO_x, VO_x, CuO_x, ...)
- Green:** Electrode materials (TiN, TaN, W, Pt, ...)

Figure 5.1: Utilizing the periodic table, RRAM materials are selected for both the top and bottom electrodes, along with metal oxide (memristive) materials. Electrodes are represented in blue, while binary oxides are depicted in red, and (perovskite type) ternary oxides are presented in green.

One of the key advantages of ReRAM is its compatibility with the CMOS fabrication process and materials, making it energy-efficient and cost-effective to manufacture [34]. These devices can operate in both unipolar and bipolar modes, with the forming process essentially representing a controlled breakdown of the oxide material. This behavior has been observed in numerous materials, including group IV and III-V semiconductors, as well as organic compounds [34]. Figure 5.1 provides an overview of materials

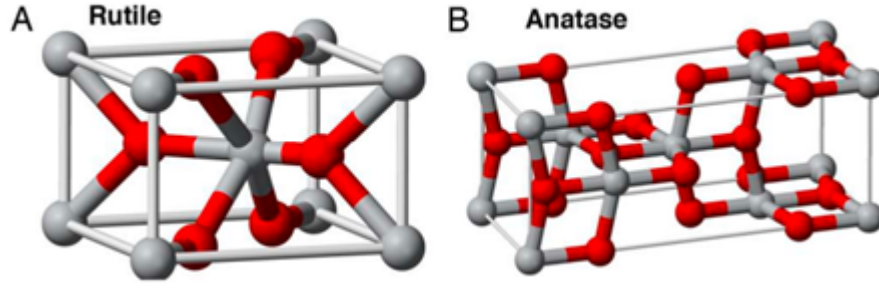


Figure 5.2: Unit cell of a) rutile and b) anatase phase of TiO₂ lattice structure. Red spheres represent oxygen and white spheres represent Ti atom.

commonly used in RRAM devices and illustrates potential options for top and bottom electrodes, along with the transition material within a memristor structure [35].

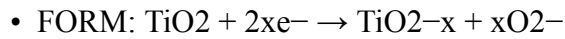
A range of materials has been utilized as the transition metal-oxide element in resistive switching memories, featuring thicknesses spanning from 2 to 130 nm. Examples encompass Al₂O₃, NiO, TiO₂, TiO_x, TaO_x, CuO_x, ZnO, and ZnO₂ [34]. To enhance the performance of ReRAM switching, it's important to optimize both the top contact and the transition material, as well as regulate the SET current. The top electrode must meet specific criteria, such as resistance to oxidation, a high work function, and ease of fabrication. According to [34], Platinum (Pt) and Silver (Ag) fulfill these requirements and are commonly used. An ideal choice for the transition metal-oxide material should possess characteristics like high ionic conductivity, straightforward manufacturing, a high Schottky barrier height, reliability at elevated temperatures, and the ability to maintain multiple stable oxidation states. TiO₂ is a frequently utilized material for this purpose [34, 36].

5.1. TiO₂-Based Memristors

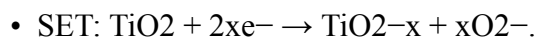
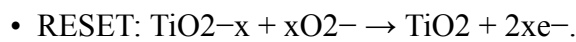
The pioneering development of the memristor based on titanium dioxide was first presented by HP Labs [5, 19] and it stands as the most widely recognized and frequently cited memristor configuration. Various research groups have also replicated this structure with certain modifications. Notably, different materials have been chosen for the electrodes in some instances. In the subsequent discussion, we will briefly explore some of the more prevalent variations of this memristor design. This particular memris-

tor type comprises a slender titanium dioxide layer situated between platinum contacts, with one side of the TiO₂ layer exhibiting oxygen deficiencies as shown in Figure 3.1 [37]. Essentially, pure TiO₂ behaves as a proficient semiconductor, featuring a 3.0/3.2 eV bandgap. However, when subjected to heat, some of the oxygen atoms evacuate the structure, resulting in the emergence of oxygen vacancies within the lattice. This phenomenon leads to a substantial decrease in the material's resistivity. In simpler terms, it transitions into a metallic state, becoming an excellent conductor, which explains its application in oxygen sensors. Notably, removing as little as 0.1% of the oxygen from TiO₂ (yielding TiO_{2-x}) is sufficient to confer substantial conductivity. These oxygen vacancies effectively serve as n-type dopants or positively charged ions capable of facilitating charge movement [38]. By applying a voltage across the memristor, lasting alterations take place within the oxide layer through a process known as electro-reduction, resulting in the formation of conductive filaments. This step is referred to as “forming” after which the memristor becomes operational.

In accordance with a device operation classification proposed by Kwon et al. [39], we can identify three distinct phases: FORM, SET, and RESET. In the initial FORM stage, a reduction of TiO₂ to TiO_{2-x} is necessary to establish the memristor's configuration. This process can be represented as follows:



As a consequence of altering the distribution of oxygen vacancies (O₂⁻) within the TiO₂ nano-layer, there is a corresponding change in resistance. This represents the initial SET operation, which is the first and irreversible cycle, commonly referred to as “forming.” Subsequently, in the RESET and SET cycles, the reactions occur as follows:



This series of operations underscores the significance of any material or combination of materials that can influence the barrier height at the interface between the top electrode and TiO₂. Such factors play a critical role in shaping and ensuring the uniformity of the switching characteristics exhibited by the memristor device.

6. EXPERIMENTAL TECHNIQUES

6.1. Sample Preparation And Measurements Techniques

In this study, the top and bottom electrodes have been deposited by RF/DC magnetron sputter, The metal-oxide layer TiO₂ was grown by using PLD technique production. Crystal structure of samples have executed by XRay diffraction (XRD) method. The thickness, density, and surface roughness of the films were controlled by the X-ray Reflectivity (XRR) technique by the Rigaku XRD device. The stoichiometry and the oxidation degree of films were analyzed by X-ray Photoelectron Spectroscopy (XPS). Electrical measurements have been measured by using a Keithley 2400 sourcemeter at room temperature including memristive resistance switching of current–voltage curves, and synaptic functions such as spike-time-dependent plasticity (STDP), long-term potentiation (LTP), long-term depression (LTD), and endurance characteristics for the memristor devices.

6.1.1. RF/DC Magnetron Sputtering

RF/DC magnetron sputtering is a widely used thin-film deposition technique in materials science and manufacturing. It involves the physical process of sputtering, which is the ejection of material atoms from a target surface and their deposition onto a substrate to create a thin film. Firstly, a vacuum chamber is used to create a low-pressure environment. Inside this chamber, there are two primary components: a target material and a substrate. The target material is typically the material you want to deposit as a thin film, while the substrate is the surface on which the film will be deposited. Inside the RF/DC magnetron chamber there is a magnetron which is a device that generates a magnetic field to trap electrons and increase the efficiency of sputtering. This configuration enhances the plasma generation and ionization of sputtered material, allowing for more controlled and uniform film deposition. In RF/DC magnetron sputtering, both radio frequency (RF) and direct current (DC) power sources are used. RF power is applied to the target material, creating a high-frequency oscillating electric field that enhances the ionization of the sputtered material. DC power is applied to the substrate to control

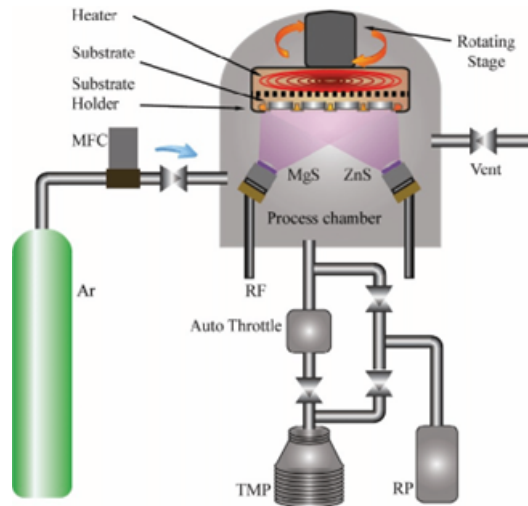


Figure 6.1: Schematic of RF/DC magnetron sputtering.

its voltage and potential, aiding in the attraction and deposition of sputtered material. When RF power is applied to the target, it ionizes the gas in the chamber, creating plasma. This plasma consists of high-energy ions and electrons. The magnetic field from the magnetron traps the electrons and increases their interaction with the target material, facilitating sputtering. And the sputtered material atoms are ejected from the target and are attracted to the substrate due to the electric potential difference created by the DC power source. As these atoms land on the substrate surface, they accumulate and form a thin film with a precise control of film thickness, composition, and other properties (Figure 6.1) [40]. So this technique offers several advantages, such as good adhesion, high deposition rates, and control over film properties. It is also possible to sputter a wide range of materials, including metals, semiconductors, and insulators and its employed in a range of applications, including the manufacturing of integrated circuits, solar cells, optical coatings, and decorative films, among others.

6.1.2. PLD Technique

Pulsed Laser Deposition (PLD) is a versatile and highly precise thin-film deposition technique relies on laser ablation as the primary mechanism for depositing thin films with excellent adhesion and minimal contamination with well-defined structures films. A high-energy laser is focused on a target material, which can be a solid, liquid, or even a composite. The intense laser pulse generates a highly energetic plasma plume con-

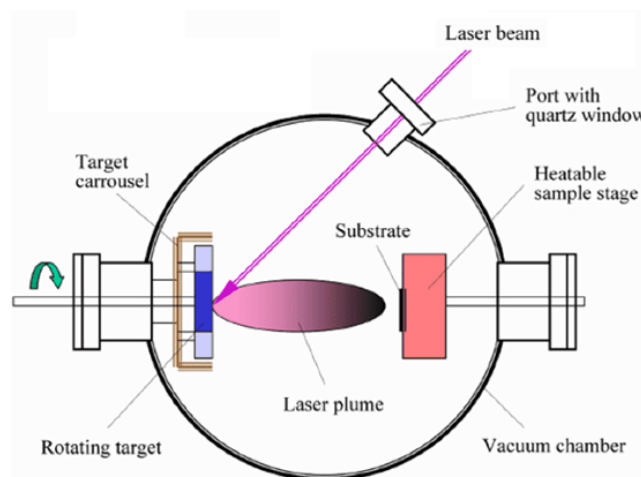


Figure 6.2: Schematic of PLD.

sisting of ions, electrons, and ablated material particles. This plasma plume expands rapidly away from the target causes localized vaporization or ablation of the target material. A substrate material is positioned in close proximity to the target material. The plasma plume containing the ablated material particles is directed toward the substrate. As the plasma plume reaches the substrate, the high-energy ions and ablated material particles collide with the substrate's surface. This results in the deposition and growth of a thin film on the substrate. The film is built up layer by layer as material from the plasma condenses on the substrate (Figure 6.2) [41]. This technique offers excellent control over the deposition process. Factors like laser energy, pulse duration, target material composition, and substrate temperature can be finely tuned to achieve precise control over film thickness, composition, and crystal structure.

6.1.3. XRD Technique

The X-ray diffraction (XRD) stands as a potent analytical method utilized for the determination of the molecular and crystal structures of materials. According to Von Laue's theory, X-ray diffraction becomes feasible when a crystal is composed of atoms arranged in a regular and scatter-centric manner, with X-ray wavelengths approximating approximately two atomic distances, typically falling within the range of 1-2 Å(angstroms) within the crystal lattice.

In 1912, William Henry Bragg and William Lawrence Bragg introduced a more math-

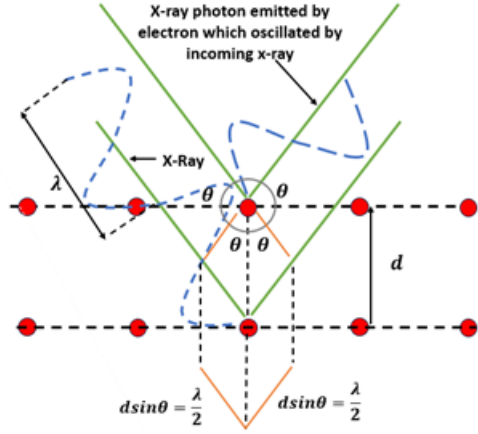


Figure 6.3: Schematics of Bragg's law [19].

ematically simplified approach to X-ray diffraction than Von Laue's concept [42, 43]. XRD can essentially be comprehended through the utilization of the Bragg equation:

$$n\lambda = 2d \sin \theta, \quad (6.1)$$

where ' n ' is an integer, ' λ ' represents the characteristic wavelength, ' d ' denotes the interplanar spacing between successive rows of aligned atoms, and ' θ ' designates the angle at which the X-ray beam interacts with the crystal lattice planes [42].

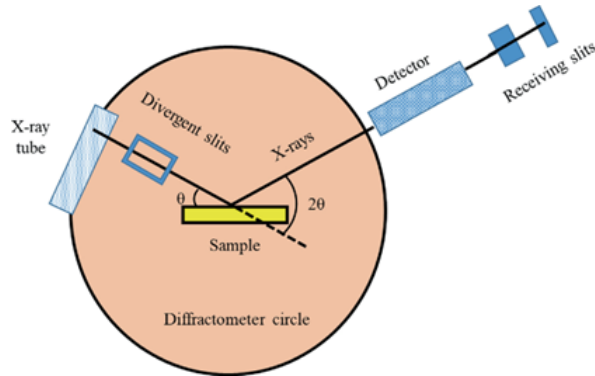


Figure 6.4: Schematic of the XRD mechanism.

When electromagnetic waves interact with a material, several outcomes can occur, including coherent scattering, the Compton effect, the photoelectric effect, pair production, and photodisintegration. For instance, as shown in Figure 6.3 [44, 45] when X-rays are directed towards a material possessing a pristine crystal structure, an interaction takes place between the X-rays and the electrons within the atoms of the crystal.

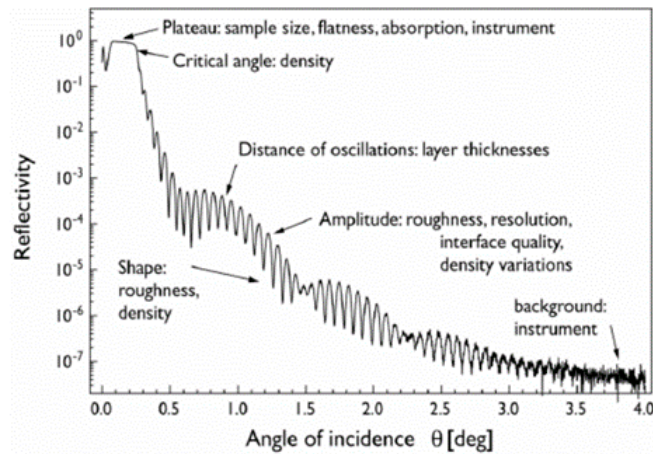


Figure 6.5: Information of the x-ray reflectivity.

This interaction causes the electrons to oscillate and emit radiation in various directions. Consequently, some of the radiation waves emitted by these oscillating electrons do not influence each other significantly. However, those waves sharing the same direction and phase exhibit constructive interference. This interference phenomenon is subsequently detected by diverse X-ray counters. In this experimental setup, a sample is positioned at an angle θ relative to the movement of the X-ray source and the moving detector. Photons are emitted from the X-ray source, and both the source and detector move at equal angles in opposite circular directions. The scattered X-rays are then captured by an X-ray counter, strategically positioned to correspond with an angle of 2θ relative to the direction of the X-ray photons originating from the X-ray source (Figure 6.4) [46].

6.1.4. XRR Technique

In contrast to X-ray diffraction (XRD), the utilization of X-ray reflectometry (XRR) doesn't require crystalline samples. Instead, it enables the determination of thickness, roughness, and mechanical density of films and film stacks within the sub-100 nm range. This analysis relies on the optical properties of X-rays, following Snellius' law. Given that layer roughness significantly influences measurement accuracy, amorphous and nanocrystalline films generally yield superior results compared to grainy polycrystalline films. The beam angles vary from the direct beam to approximately 5° , contingent on the film properties and materials involved. This technique is based on the

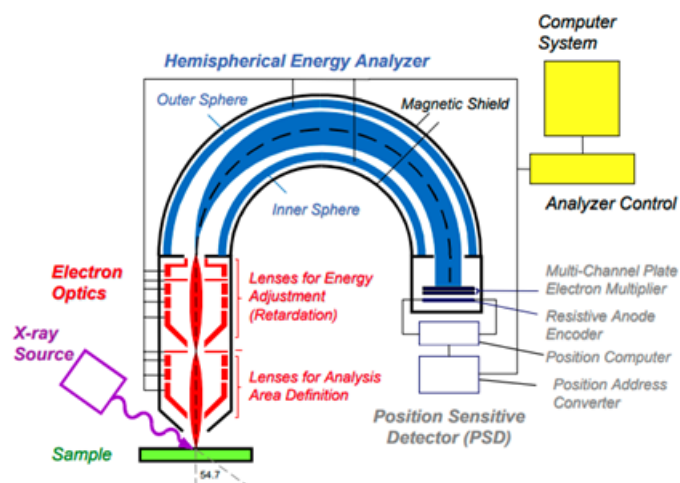


Figure 6.6: Schematic of XPS.

interaction of X-rays with a sample's surface or thin film. The experiments are typically conducted using a specialized X-ray source, such as a synchrotron or an X-ray generator, and a high-resolution X-ray detector. The sample is positioned at a specific angle relative to the incident X-ray beam. When X-rays strike the sample, they are partially reflected, and the intensity of the reflected X-rays is measured as a function of the incident angle which is systematically varied. So by measuring the intensity of the reflected X-rays at different incident angles, the technique provides information about the sample's surface and interface structure. The data obtained from the XRR experiment is analyzed using mathematical models and algorithms to extract structural parameters. The data often results in a reflectivity curve, which is fitted to a model function to determine parameters like layer thickness, electron density, and interface roughness. An XRR example has been shown in Figure 6.5 [47].

6.1.5. X-Ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) stands out as a widely used analytical technique in materials science, offering insights into the surface chemistry of diverse samples. This Primer addresses optimal practices for XPS analysis, catering to both beginners and seasoned users. The emphasis is placed on thin film samples synthesized under vacuum conditions, considering the notable surface-to-volume ratio inherent to such films. Critical factors influencing the final outcome, such as substrate selection

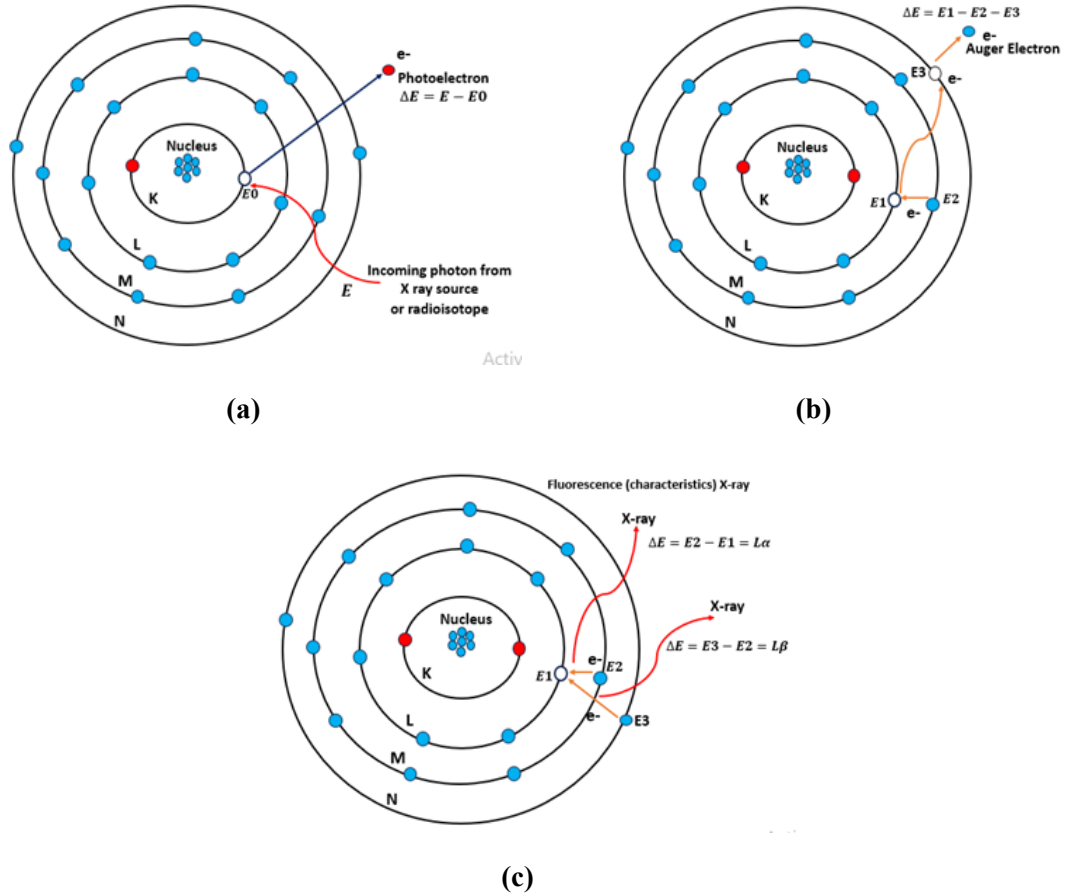


Figure 6.7: a) Occurring of the photoelectron, b) occurring of auger electron, c) emitting Fluorescence mechanism.

and air exposure duration, are explored. Key concepts, including binding energy, the photoelectric effect, spectral referencing, and chemical shift, are introduced. Figure 6.6 [48].

The process of XPS begins with the interaction of x-ray photons with the atoms in the sample. When an x-ray photon collides with an electron in an atom, it can impart enough energy for the electron to escape its orbital shell. This event is known as the generation of a photoelectron. Notably, Heinrich Hertz was the first to observe this phenomenon in 1887, while Albert Einstein provided the first comprehensive explanation in 1905. Furthermore, in another scenario, an electron can occupy the vacated orbital position in the atom, emitting an x-ray photon in the process. This x-ray photon may, in turn, interact with an electron in the outermost shell, leading to the removal of that electron. This specific type of electron is referred to as an Auger electron, a discovery

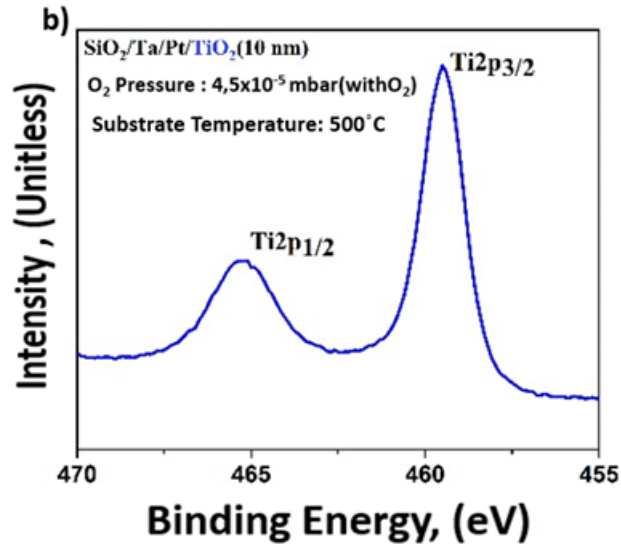


Figure 6.8: An example of XPS data TiO₂ film on software.

attributed to Lise Meitner in 1922 and Pierre Victor Auger in 1925. Additionally, XPS can yield fluorescence emissions, specifically characteristic x-rays, which are produced when high-energy electrons take the place of the removed electron within the atom as shown in Figure 6.7 [44].

In XPS, photoelectrons are generated by x-rays sent from the x-ray source to the sample. Before reaching the analyzer, these photoelectrons are focused using transfer lens 23 within the XRD mechanism. Subsequently, the focused photoelectrons enter a hemisphere analyzer, where they are compelled to move in a circular trajectory before being directed into an x-ray counter through a pair of electrodes with positive and negative potentials. The computer, equipped with XPS software, records important parameters such as the binding energies (in electron volts), kinetic energies (in electron volts), and the rate of photoelectron emission per second (CPS) Figure 6.8. These data are then used to create graphical representations, with distinctive peaks corresponding to specific elements, facilitating the identification of elemental composition.

6.1.6. Lithography Technique

For a more extensive and detailed electrical characterization, as well as the fabrication of a more intricate set of memristor devices, the development of a mask set has

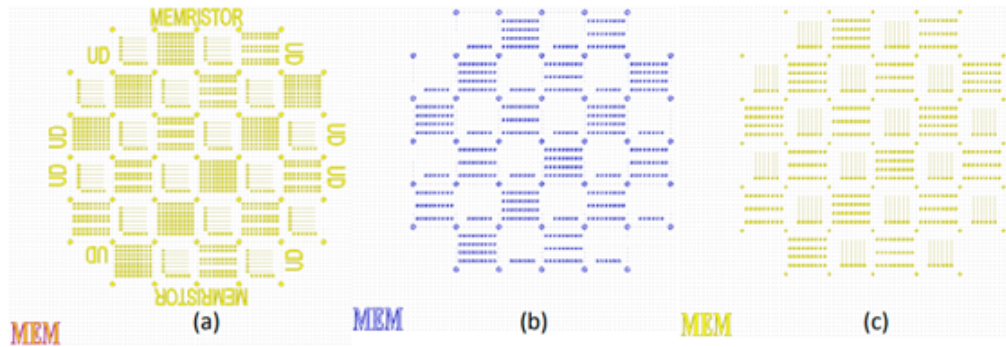


Figure 6.9: Illustrates the arrangement for (a) top metal mask, (b) etch mask, and (c) bottom metal mask.

been undertaken. This mask set plays a pivotal role in the photolithography process, crucially defining and generating intricate patterns that form the various layers of the device. Importantly, the application of this mask set facilitates the production of significantly smaller devices in terms of footprint area, including memristor crossbar arrays. Comprising three distinct masks—top metal, bottom metal, and an etch mask. The top metal mask features all probing pads, while the bottom metal mask includes only those pads connecting to the bottom electrode on the device. The etch mask serves the purpose of providing access to the bottom metal, as vias will be etched precisely where the pads connected to the bottom electrode require access from the top of the device. As an example of a mask set is illustrated in Figure 6.9 [49].

The process involves several steps, and here is a general overview of the use of mask sets in the device fabrication:

1. Photolithography:

- Purpose: Photolithography is a key process used to transfer a pattern from a photomask to a substrate, usually a silicon wafer coated with photoresist.
- Mask Set Components: The mask set consists of multiple masks, each designed for a specific layer of the semiconductor device. These masks contain the patterns that will be transferred to the wafer during photolithography.

2. Mask Creation:

- Design Process: The creation of a mask set begins with the design of each

individual mask. These designs are based on the specifications of the semiconductor device being manufactured.

- **Layer-Specific Patterns:** Each mask in the set corresponds to a specific layer of the semiconductor device. These layers may include transistors, interconnects, and other components.

3. Layer Patterning:

- **Layering Process:** During the fabrication process, the wafer undergoes various deposition and etching steps to build up the semiconductor device layer by layer.
- **Alignment:** The alignment of each layer is critical for the proper functioning of the device. The mask set ensures precise alignment of patterns from one layer to the next.

4. Memristor Devices and Mask Sets:

- **Material Deposition:** In the case of memristor devices, the mask set may involve specific patterns for the deposition of materials critical to the memristor's operation, such as transition metal oxides.
- **Electrode Definition:** The mask set will define the patterns for the electrodes that make contact with the memristor material.
- **Geometric Considerations:** Masks play a role in defining the size, shape, and critical dimensions of the memristor, influencing its electrical properties.

5. Quality Control:

- **Inspection:** The masks undergo rigorous inspection processes to ensure that they are defect-free. Even small defects on a mask can result in defects on the final semiconductor device.

7. EXPERIMENTS AND RESULTS

The metal oxide-based memristor device structures of Si/SiO₂/Ta/Pt/TiO_x/Pt, was produced using the thin film production system in Nanotechnology laboratory of Gebze Technical University (Figure 7.1). The metal oxide layer TiO_x was produced using the Pulsed Laser Deposition (PLD) system, and the Pt top/bottom electrodes were produced using the Magnetron Sputtering system. The connection system ensuring vacuum conditions links these two growth systems. Thin films have been characterized with using XPS, XRD, XRR measurement techniques in Nanotechnology Institute laboratory and DC, AC electrical and synaptic characterization have been investigated in Physics laboratory at Gebze Technical University.

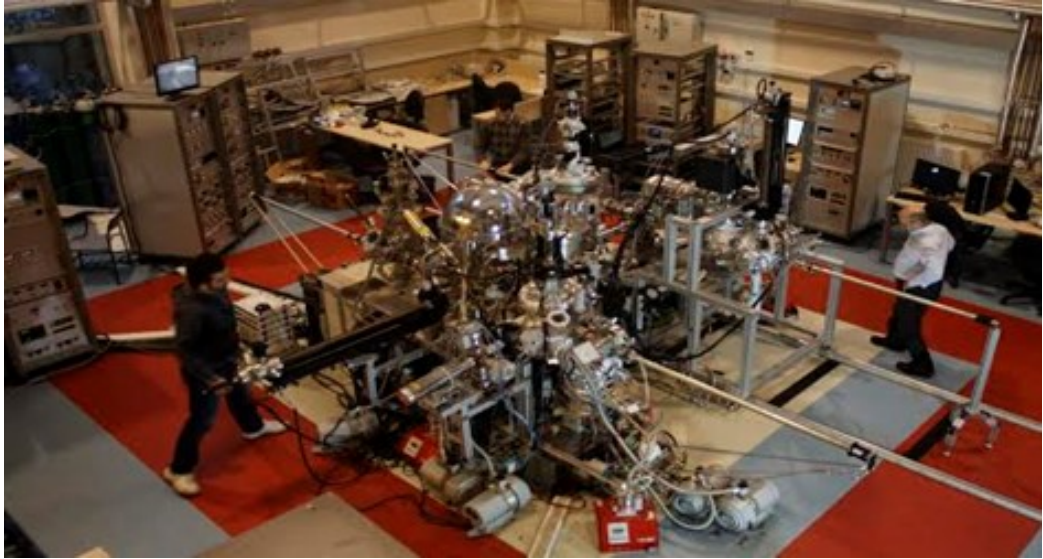


Figure 7.1: Nanotechnology Institute laboratory at Gebze Technical University.

7.1. Device Fabrication of Experiment 1

The production process proceeded as follows: The initial step involved a cleaning process, wherein the self-oxidized Si/SiO₂ substrate material underwent ultrasonic cleaning in acetone and isopropanol for 5 minutes. Subsequently, it was rinsed with deionized water, followed by heating at 400 °C for 15 minutes in the magnetron sputtering system's heating apparatus to eliminate any residual alcohol contamination on the sur-

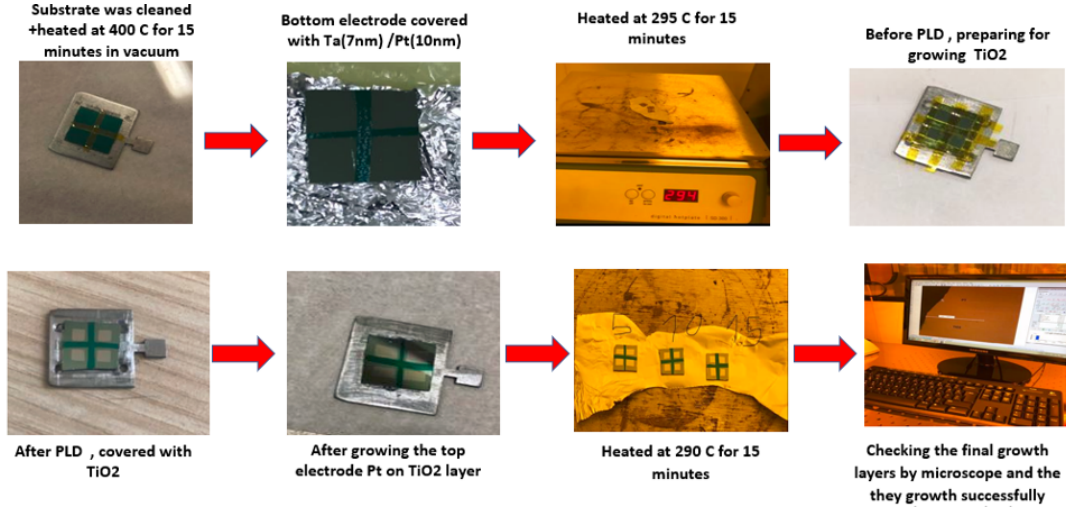


Figure 7.2: Production process of the memristor device in Si/ SiO₂/ Pt/ TiO_x (5, 10, 15) nm/Pt structure.

face. The electrode deposition occurred through RF/DC magnetron sputtering at a base pressure of 10^{-9} mbar (UHV). All polished surfaces of 10 mm x 10 mm SiO₂ substrates were coated with Ta(7nm)/Pt(10nm) for the bottom electrodes (BE). The growth process took place for 15 mins and 15:09 mins, respectively, utilizing Ta as an adhesion layer between Pt (bottom electrode) and SiO₂. Following the production of the bottom electrode, the structure was heated again in an atmosphere at approximately 295 °C for 15 minutes to form a more stable film structure. The Pt top electrodes (TE) were fabricated with a surface area of 0.5 mm x 0.5 mm.

The TiO_x metal oxide layer was produced in a vacuum system using the PLD system. A KrF ($\lambda=248$ nm) excimer pulsed laser source was employed for thin film deposition. The pulsed KrF excimer laser beam, focused on the TiO₂ target at a 45° incidence angle, was emitted at a repetition rate of 2Hz, power of 250mJ, and laser fluence of $2.4 J/cm^2$. The PLD process durations were 172 sec, 75 sec, and 37 sec, resulting in TiO_x thin films with thicknesses of nearly 15 nm, 10 nm, and 5 nm, respectively.

Subsequently, the structure was transferred back to the magnetron sputtering system to grow the top electrode Pt (20 nm) on the metal oxide layer. Similar to the Pt bottom electrode growth process, the structure underwent heating again at approximately 290 °C for 15 minutes in an atmosphere after the Pt top electrode was grown to ensure an ideal film structure. The entire device production process is shown in Figure 7.2.

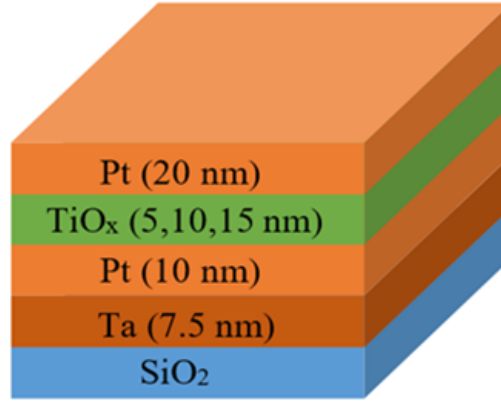


Figure 7.3: Single-cell memristor thin films prepared in Si/SiO₂/Ta/Pt/TiO_x/Pt stack structure.

Using the magnification processes described above, single-cell memristor devices have been prepared. The structural and electrical characterizations of these devices are presented in the relevant sections.

7.1.1. Structural Characterization

7.1.1.1. XRR

Surface roughness of the bottom/top electrode, thickness, and physical density and metal oxide layer in the resulting film were accurately determined using the X-Ray Reflectivity (SA-XRR) technique. The measurements were conducted using the Rigaku XRD device with a CuK α X-ray source ($\lambda = 0.154\text{nm}$) at room temperature. Figure 7.4 shows the XRR graph of the SiO₂/Pt/TiO₂ structure we prepared, which shows both experimental and simulation results. The fitting parameters of the thickness, density, and surface roughness of the layers are shown in Table 7.1. Based on the analysis, the Pt electrode thickness was determined to be 10 nm and the TiO_x layer thickness was 13.5 nm. These values were used for device calibration to achieve the desired thickness of each layer in the device.

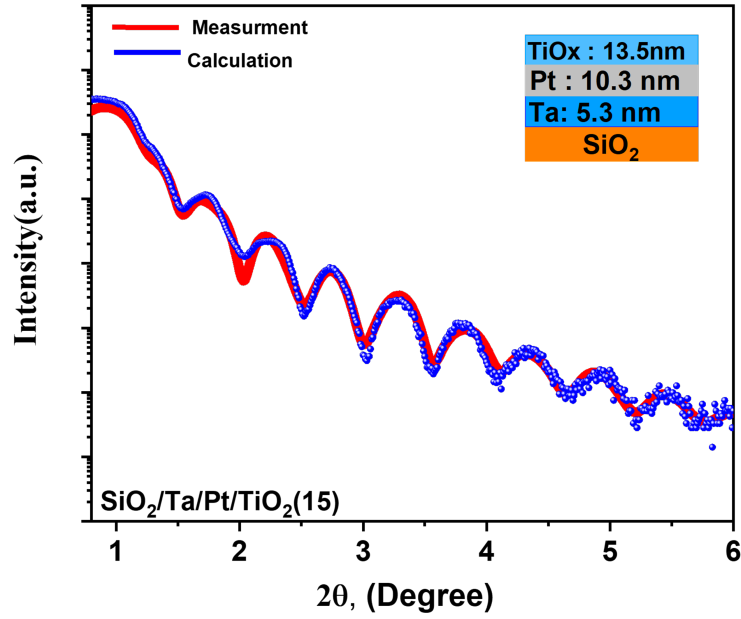


Figure 7.4: Small angle X-ray reflection (XRR) results of the memristor device with SiO₂/Ta/Pt/TiO_x/Pt structure. Blue line show experimental data, and Red line shows simulation result. As a result of the simulation, the thickness, physical densities and roughness of each layer are shown in a table.

Table 7.1: XPS fitting parameters of SiO₂/Pt/TiO_x (13.5nm).

ID	Material	Thickness (nm)	Density (g/cm ²)	Roughness (nm)
4	TiO ₂	13.5	3.57(11)[-]	0.62
3	Pt	10.322	21.43(11)[-]	0.368
2	Ta	5.278	15.1(3)[-]	0.8
1	SiO ₂	187.219	2.2[-]	0.5
Sub.	Si	0	2.33[-]	0.5

7.1.1.2. XRD

According to the results of XRD in Figure 7.5 rutile peaks have been detected as shown in the figure. Where In Figure 7.5a, we investigated the impact of an elevated temperature on the crystal structure of the thin film TiO₂ under atmospheric conditions. This involved subjecting the TiO₂ thin film to a annealing process at 900°C in ambient atmosphere. The results revealed five distinct TiO₂ peaks, indicating the presence of both rutile and anatase phases, as illustrated in the figure.

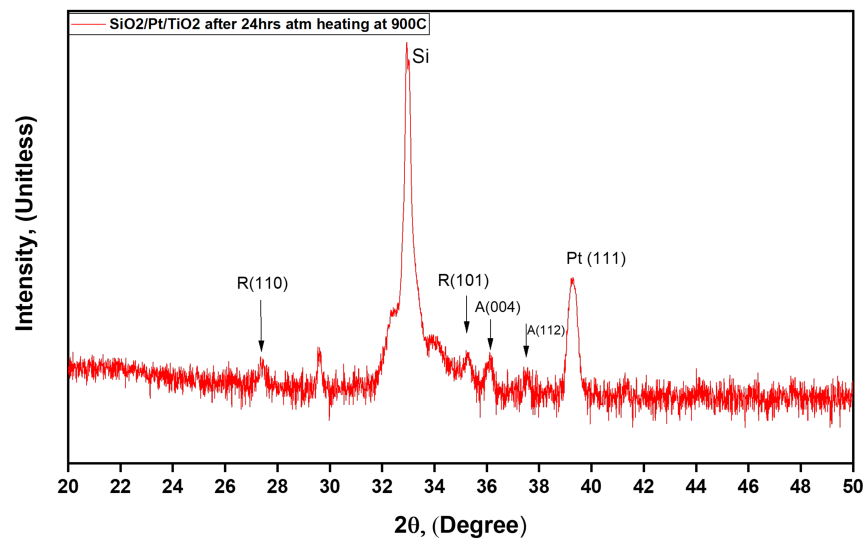


Figure 7.5: XRD result of SiO₂/Ta/Pt/TiO₂ thin film.

7.1.1.3. XPS

Figure 7.6 shows the X-ray Photoelectron Spectroscopy (XPS) result indicating the stoichiometry and bond formation of metal ions with oxygen ions in the grown TiO_x metal oxide layer to obtain detailed information about the structure. XPS data were obtained using an Al K α radiation ($h\nu = 1486.6$ eV). The XPS spectra demonstrate the formation of rutile TiO₂ structure. The measurement was done precisely by focusing on the binding energies of Ti and O elements within the sample. Based on the outcomes of the simulation, the resulting XPS curve reflects contributions from both Ti⁴⁺ and Ti³⁺.

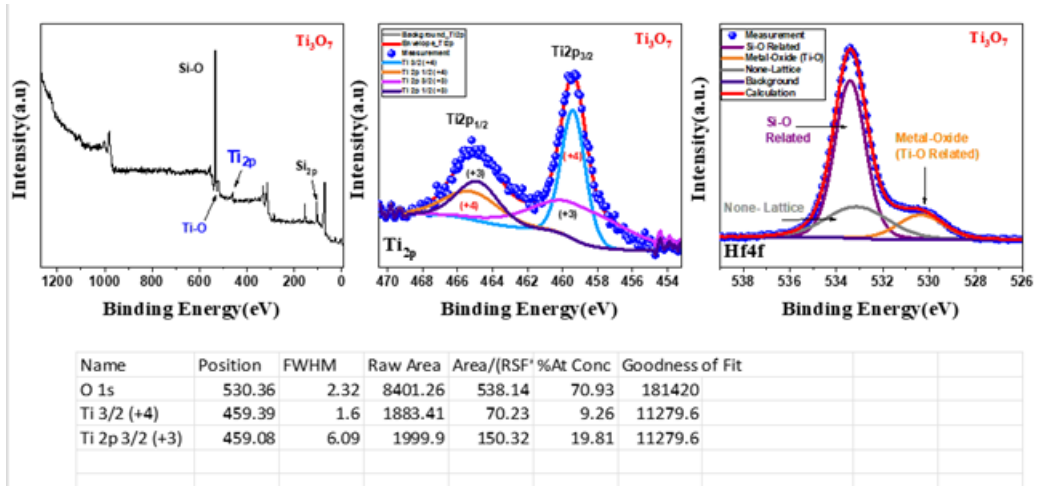


Figure 7.6: Experimental and theoretical X-Ray Photo-electron spectroscopy (XPS) peaks of Ti and O in for samples with SiO₂/Ta/Pt/TiO_x/pt structure.

The Ti⁴⁺ peaks align consistently with those expected for Ti⁴⁺ in TiO₂, while the presence of Ti³⁺ ions is attributed to broken bonds at the surface and oxygen deficiencies in deeper layers. The O1s spectrum's best fitting indicates that the observed peak originates from both lattice and non-lattice oxygen, with respective binding energies of 530 and 533 eV. These fit values and binding energies are in line with existing literature, confirming the formation of TiO₂. Notably, the relatively higher abundance of Ti⁴⁺ compared to Ti³⁺ in the spectrum provides clear evidence of the growth of the TiO₂ film, with Ti³⁺ ions associated with the reduction of TiO₂ to TiO_x. XPS peaks belonging to Ti element are observed as two separate peaks at around 460 and 466 eV due to the spin-orbit interaction. The weaker peak belongs to p_{1/2} and the other one belongs to p_{3/2} orbitals.

7.1.2. Electrical Characterization

7.1.2.1. I-V Curve Characterization

Electrical measurements using DC scanning the current-voltage (I-V) curves were measured and the results are presented in Figure 7.7 where Current-voltage (I-V) curves were measured after applying a forming process to the samples at a voltage of + 1V, 2V, 4V for 4 ms prior for samples with TiO₂ thicknesses of 5 nm, 10 nm, and 15 nm respectively using triangular voltage for about 10 seconds after the forming process. And

as we can see all devices display the pinched hysteresis shape and resistive switching characteristic.

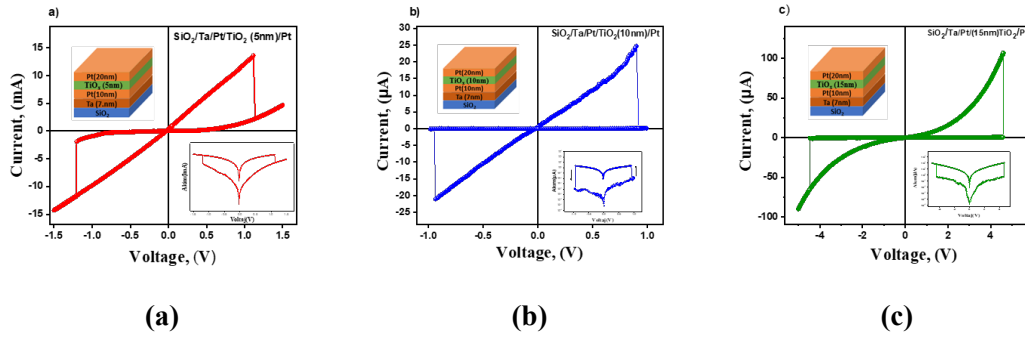


Figure 7.7: The current-voltage characteristics for TiO₂-based memristor devices with different thicknesses: a) 5 nm TiO_x device, b) 10 nm TiO_x device, c) 15 nm TiO_x device.

As shown in Figure 7.7 when the voltage sweeps from 0 to approximately +1.2 V in 5nm TiO_x layer device. The device undergoes a transition from a state of low resistance (LRS) to high resistance (HRS), creating a non-volatile 'OFF' state during the RESET process. The high resistance state remains stable even after applying negative voltage until the negative voltage attains a specific threshold, prompting a transition from HRS to LRS. This transition leads to the establishment of an 'ON' state through the SET process, and same thing happens for the two other devices with their different threshold voltage sweeps. The differences in current results between TiO₂ films with different thicknesses in our memristor devices can be attributed to several factors related to the physical properties and behavior of thin films. For example, in the case of 5nm thick TiO₂ film results in higher current compared to the other thicker devices and that can be contributed to quantum confinement effects where in thinner films might have lower potential barriers for charge carriers, allowing for more efficient tunneling through the film leading to higher current flow compared to thicker films where tunneling might be less probable. On the other hand, we can see that by increasing thickness from 10 nm to 15nm a higher current is achieved as it shown in the figures, and this can be contributed to that fact that 15 nm films may have a more controlled and predictable behavior in terms of oxygen vacancy migration, leading to better control over resistance

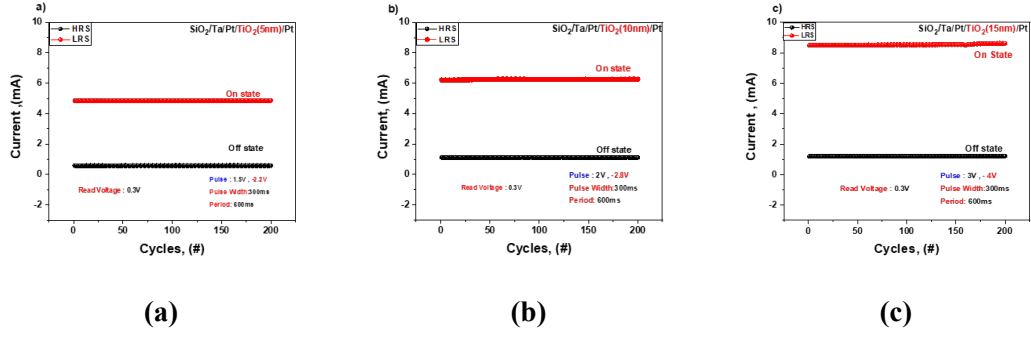


Figure 7.8: Endurance characteristics for TiO₂-based memristor devices with different thicknesses. a) Memristor device with 5 nm TiO₂ thickness, b) 10 nm TiO₂ thickness, c) 15 nm TiO₂ thickness.

states and potentially higher currents compared to that in 10 nm thick. It's important to note that the behavior of memristor devices is a complex interplay of various material and design factors. The specific reasons for the observed differences would depend on the detailed characteristics of the devices, the fabrication process, and the specific properties of the TiO₂ thin films used. Experimental analysis and detailed studies of the electrical characteristics would be necessary to provide a more definitive explanation in a particular case. Also, our I-V measurement results indicate that the memristor structures in the produced thin films have a wide hysteresis shape indicates a larger range of resistance changes in response to applied signals so the device can be utilized as a digital information storage device which can be advantageous in certain applications where a broader spectrum of resistance values is desired for encoding information or for simulating complex neural behaviors in neuromorphic systems. Furthermore, the IV characteristics for 5 and 15 nm TiO₂ samples demonstrates that a greater applied voltage is necessary to transition the structure from a high resistance state (HRS) to a low resistance state (LRS) and vice versa when dealing with thicker TiO₂ layers.

7.1.3. Characterizing Synaptic Plasticity Performance

The correlation between a memristor and a synapse stands out, particularly when examining the Hudgin-Huxley neuron model, recognized with the 1961 Nobel Prize in physiology. Within this model, the sodium and potassium ion channels in an axon dis-

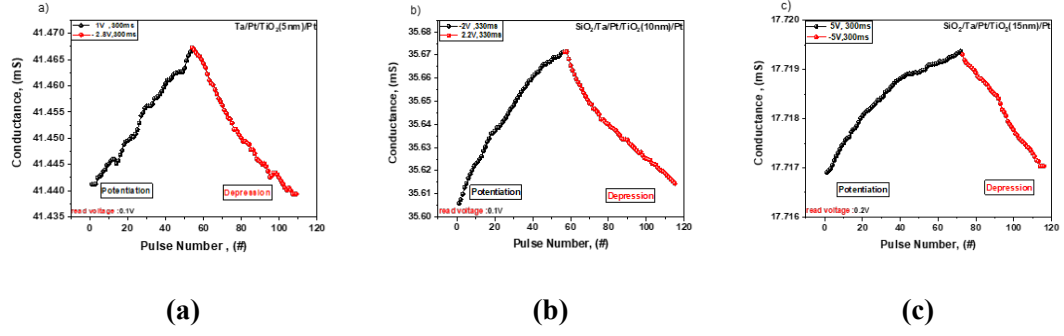


Figure 7.9: Potentiation and depression by applying AC pulse. Measured potentiating (1st pulse to 60th pulse) and depressing (61st pulse to 120th pulse) curves of the Si/SiO₂/Ta/pt/TiO_x/pt devices. a) Memristor device with 5 nm TiO₂ thickness, b) 10 nm TiO₂ thickness c) 15 nm TiO₂ thickness.

play time-varying conductance, serving as examples of memristive devices[50]. Neuroplasticity governs the human brain's neural network, allowing it to form robust or weak connections. Nonlinearities in neuron function arise from the action potentials it receives, and the memristor emerges as a physical device adept at replicating these nonlinear patterns. Several studies suggest that memristor systems can carry out synaptic functions such as spike timing-dependent plasticity, short-term memory (STM), and long-term memory (LTM) transitions. Dynamic data processing involves short-term effects, including STP and STD spikes[51–53]. Each synapse engages in intricate signal processing, aligning with the objectives of neuromorphic architectures seeking to emulate brain functions. In comparison, while current microprocessors achieve densities of around 10^9 square centimeter, human synapses are densely packed with ten times more density 10^{10} per cm². Motivated by the brain's neurotransmission, memristors, with their inherent resistive switching capabilities, emerge as promising candidates for mimicking both artificial synapses and neurons[54–56]. These devices showcase an impressive switching performance matrix, featuring long retention (>10 years) [57], stable endurance greater than 10^{10} cycles[58], minimal switching energy consumption [59, 60], fast switching speed (<1ns)[60, 61], and nanoscale cells (<10nm)[60].

7.1.3.1. Retention Measurement Results

The retention properties of memristors play a crucial role in achieving memory devices with exceptional stability, as well as in the development of neuromorphic or synaptic devices. Figure 7.8 shows the data retention characteristics of 5, 10, 15 nm TiO_x devices where The retention behaviors of the memristor were tested at room temperature for a duration of 200 cycles for 42 minutes and a read voltage of 0.3 V for all devices . Here, pulsed biases were utilized to program the low resistance state (LRS) and high resistance state (HRS) of the system. of -2.2 V and 1.6 V for 5nm TiO_x device. For 10 nm device -2.8V and 2V. And for 15nm -4V and 3V respectively. (pulse widths and period were 300ms and 600 ms respectively for all 3 devices). The results shows that the three devices showed stable operation up to 200 cycles without a considerable change in the current levels of ON (ION) and OFF (IOFF) states. Furthermore, Despite changes in the current level of the LRS based on the SET voltage, the current level of the HRS remained constant. Consequently, the current ratio for each sample was altered, revealing that an increase in the pulse voltage of the samples resulted in a wider current ratio and this is consistent with the literature[62].

7.1.3.2. LTP and LTD Measurement Results

The symmetry in the update characteristics of synaptic weights between long-term potentiation (LTP) and long-term depression (LTD) is a critical factor in the design of synaptic devices. It directly impacts the learning accuracy of neuromorphic computing [63, 64]. As shown in Figure 7.9 conductance changes in response to programming pulses are illustrated. Upon the application of a series of sixty identical pulses—positive potentiating (P) pulses followed by subsequent negative depressing (D) pulses—the device’s conductance exhibits a gradual increase (depicted in black) and decrease (depicted in red), respectively. Consequently we measured the long-term plasticity of the devices using varying voltage conditions. For the 5nm configuration, the VPOT was set at +1 V during the potentiation process, while the VDEP was adjusted to -2.8 V. In the case of 10 nm, the VPOT was maintained at -2 V for potentiation, with VDEP varied at 2.2 V. For the 15 nm setup, the VPOT was set at +5 V during potentiation, while the VDEP was set at -5 V. Each potentiation and depression

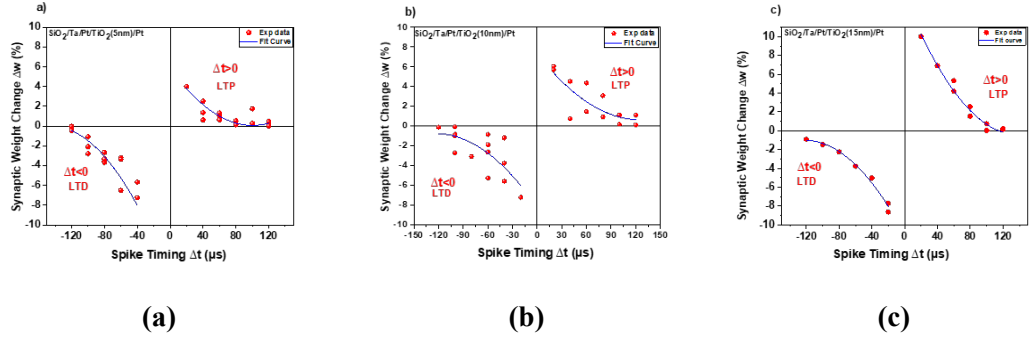


Figure 7.10: Spike timing-dependent plasticity (STDP) with the structure of Si/SiO₂/Ta/pt/TiO_x/pt the relationship between the relative change of the memristor synaptic weight (Δw) and the relative spike timing (Δt). And the solid line is the exponential fitting curve to the experimental data. a) Memristor device with 5 nm TiO₂ thickness, b) 10 nm TiO₂ thickness c) 15 nm TiO₂ thickness.

cycle consisted of 60 repetitions. The pulse width of each pulse was 300 ms and the pulse interval was 305 ms and the read voltage was 0.1V for 5 and 10 nm TiO_x devices, and 0.2V for 15nm TiO_x device. The conductance of the device was measured following each programming pulse. Consistent with the DC characteristics of the device, the application of potentiating voltage pulses systematically enhances the memristor's conductance, while the application of depressing voltage pulses systematically reduces the memristors conductance.

7.1.3.3. STDP Measurement Results

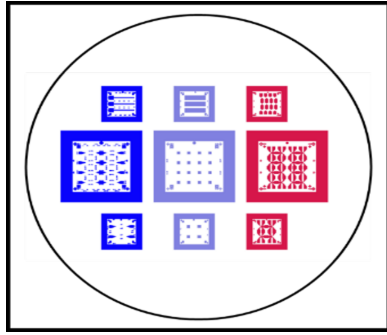
Figure 7.10 shows the Experimental results for spike-time-dependent plasticity. Here Δt represent relative timing between pre- and postsynaptic neuron ($\Delta t = t_{post} - t_{pre}$). When the presynaptic neuron fires before the postsynaptic neuron ($\Delta t > 0$) it results in Long-Term Potentiation (LTP). Conversely, if the postsynaptic neuron fires before the presynaptic neuron ($\Delta t < 0$).Long-Term Depression (LTD) occurs. The change in synaptic weight, denoted as Δw , is expressed as $\Delta w = 100\%(I_1 - I_0)/I_0$, where I_0 and I_1 are the Current after pre- and postsynaptic spikes, respectively [65]. The findings indicate a robust correlation between the changes in synaptic weight Δw and the variations in spike timing Δt where Δw of LTD and LTP will decrease with

the increase of the Δt . Observing the device with a 5 nm thick oxide layer, we note that the Δw change was comparatively smaller than in the other two devices. We posit that the thickness of the oxide layer significantly influences the synaptic performance of these devices, as evidenced by the observed changes. Furthermore, the modifications in synaptic weight suggest the effectiveness of our TiO₂-based memristor devices in functioning as artificial synapses.

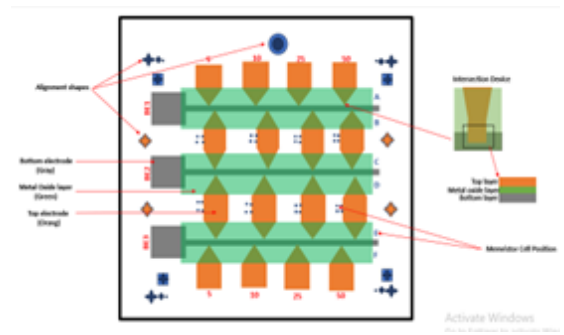
7.2. Device Fabrication Experiment 2

7.2.1. Lithographic Processes of Fabricated Device

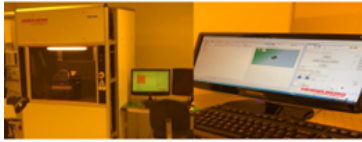
The text describes the lithographic processes for single-layer memristor devices with different surface areas using the photolithography method. In this scope, the mask printing process for single-cell devices was carried out as illustrated in Figure 7.11(a). The mask was created using the CleWin5 computer program. A total of 24 memristor cells, with surface areas of 5×5 , 10×10 , 25×25 , and $50 \times 50 \mu\text{m}^2$ each, were printed onto a $10 \times 10 \text{ mm}^2$ region. The prepared mask, detailing 24 memristor devices, is shown in detail in Figure 7.11(b). The mask model for memristor devices, designed using the CleWin5 software, was transferred onto a chrome mask using the HEIDELBERG-dwl666fs laser lithography system, as shown in Figure 7.11(c). The surfaces of the chrome masks are coated with a positive photoresist coded as AZ1505. Figure 7.11(d). Figure 7.11(e) illustrates the printing of the mask model onto the chrome mask using calibrated parameters for the AZ1505 photoresist in a Heidelberg laser mask writer. Following the printing process, the mask was exposed to light after being immersed in AZ726 MIF developer chemical for 55 seconds, as shown in Figure 7.11(f-g) and the designed chrome surface was revealed by removing the positive photoresist-coated areas from the mask. Immediately after the development chemical process, the revealed pattern was subjected to chrome etching in chromic acid under room conditions for 100 ± 10 seconds, resulting in the exposure of the glass surface devoid of chrome. As a result of the chrome etching process, the chrome mask was made ready for use in lithography, as depicted in Figure 7.11(h).



(a)



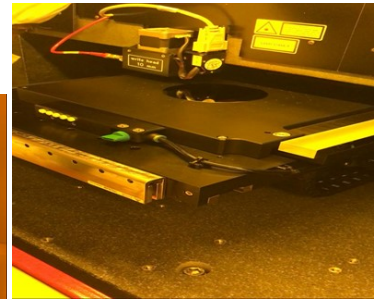
(b)



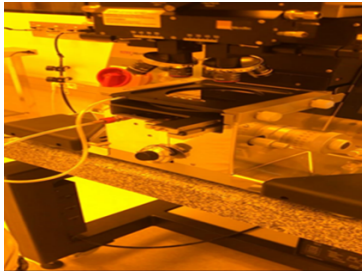
(c)



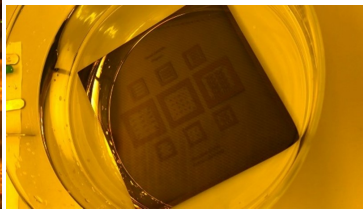
(d)



(e)



(f)



(g)



(h)

Figure 7.11: a) The mask design for the production of the bottom electrode layer (Blue), metal-oxide layer (Purple), and top electrode layer (Pink) for the memristor devices, b) The design includes single-cell memristor devices with different surface areas (5×5 , 10×10 , 25×25 , and $50 \times 50 \mu\text{m}^2$), with 6 cells each, totaling 24 memristor cells in a $10 \times 10 \text{ mm}^2$ area, c) HEIDELBER–dwl666fs laser lithography system, d) Spin coating with positive photoresist, e) Heidelberg dwl666fs control panel and printing process, f) mask was exposed to light, g) Development process of the mask in AZ726 MIF chemical, h) Chrome mask ready for lithography after chrome etching.

7.2.2. Layers Growth Processes of Fabricated Device

Single-cell memristor devices with a sandwiched single-layer metal oxide layer between two metal electrodes on a SiO₂ substrate are represented in Figure 7.12. A three-layer photolithography method is used for the fabrication of the produced memristor devices. The lithography parameters are the same for each layer. Prior to the lithography process, SiO₂ substrates are cleaned of surface impurities by vibrating them in an ultrasonic bath with acetone, isopropyl alcohol, and deionized water for 10 minutes each. The cleaned substrates are dried with nitrogen gas and then heated at 200°C for 15 minutes at atmospheric environment. The prepared substrates are coated with AZ1505 photoresist using the parameters of 4000 rpm and heated for 55 seconds.

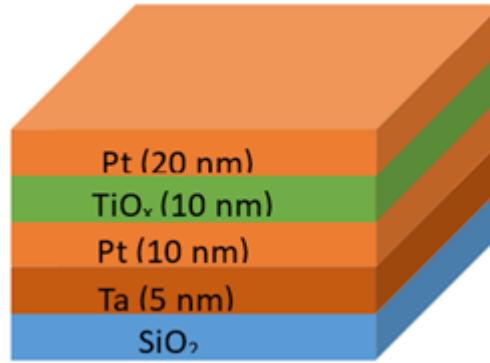


Figure 7.12: Single-cell memristor thin films prepared in Si/ SiO₂/ Ta/ Pt/ TiO_x(10)nm/Pt stack structure.

After the coating process, alignment was performed using the mask alignment Device at Gebze Technical University Nanotechnology Laboratory, followed by exposure to a mercury lamp with a wavelength of 365 nm for 0.5 seconds. Following the exposure process, a pattern was created by removing the photoresist areas exposed to light using the AZ726 MIF developer chemical, and the substrate was prepared for the production of the bottom electrode. The same processes were sequentially carried out for the metal-oxide layer and top electrodes. In order to mature the growth conditions on the SiO₂ substrate, a 5 nm thick layer of Tantalum (Ta) was grown before the Platinum (Pt) bottom electrode.

In the structure of the memristor device, bottom electrodes were sequentially grown

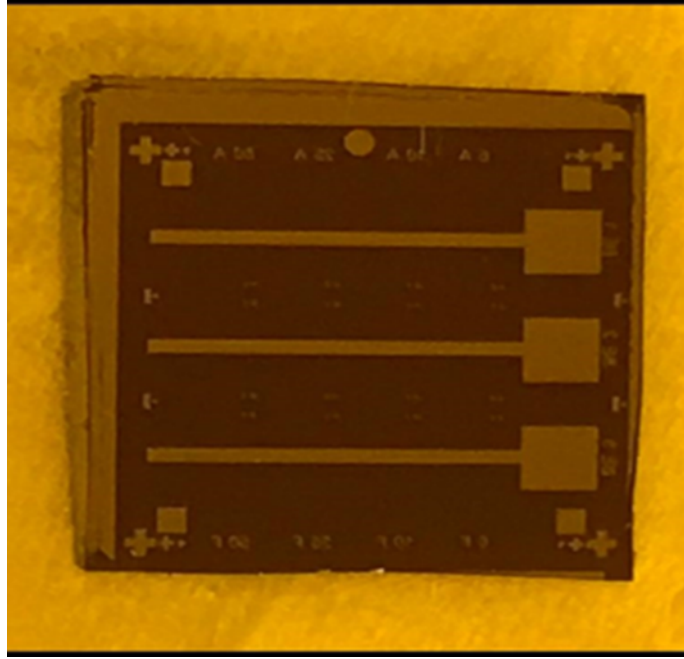


Figure 7.13: Bottom electrode lithography.

as Si/SiO₂/Ta/Pt/10nm thick Ta/Pt respectively, and top electrodes were grown as 20 nm thick Pt. The deposition of Ta/Pt thin film was carried out using the DC sputtering method under room temperature conditions, with a scattering power of 10 W and an Ar pressure of 5×10^{-3} mbar. After the growth of Ta/Pt bottom electrode and Pt top electrode films, the removal of photoresists was achieved using acetone. At this stage, the films were annealed in the atmospheric environment at 200°C for 20 minutes to enhance the electrode durability. In the structure of the memristor device, the active layer (metal-oxide layer) composed of TiO₂ thin film was produced using the Pulsed Laser Deposition (PLD) method through a lithographic process. In the production process, a pulsed laser based on KrF with a wavelength of 248 nm, was utilized. The device parameters calibrated for the metal oxide TiO₂ thin film were as follows. The PLD device operated in EGY NGR mode, and laser pulses with a frequency of 10 Hz and a laser pulse power of 3 W were focused on the sample through an appropriate lens path. The energy generated by the laser on the sample was calculated to be 300 mJ. Film production took place in an oxygen-free environment at room temperature for 1 minute and 12 seconds. As shown in Figure 7.14, after the production of the top electrode, the device was prepared for characterization.

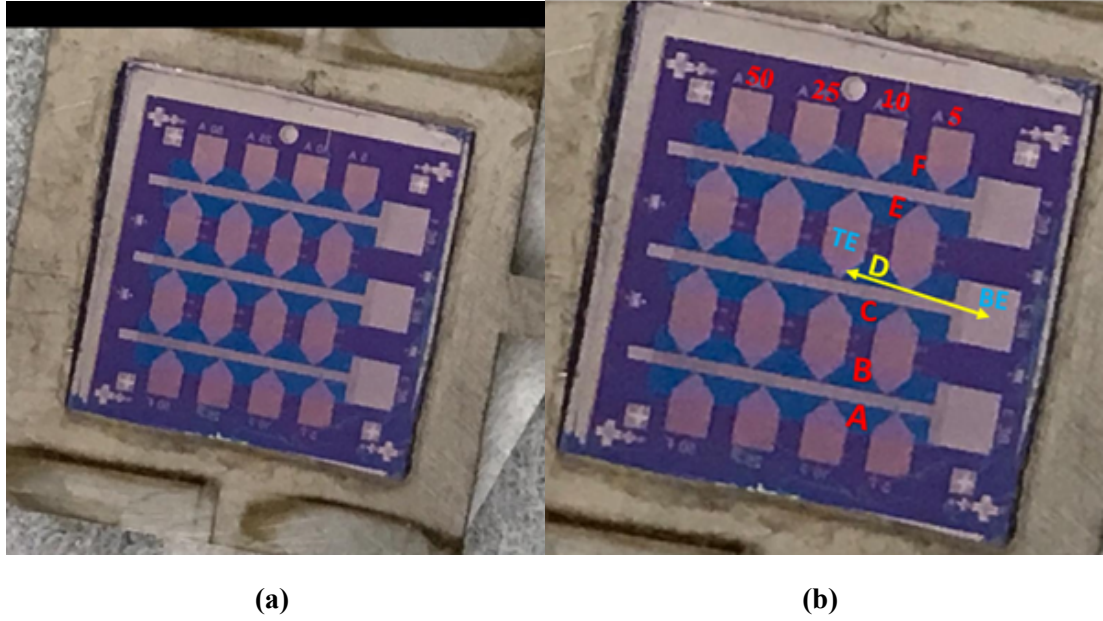


Figure 7.14: Device produced under room conditions in the PLD system.

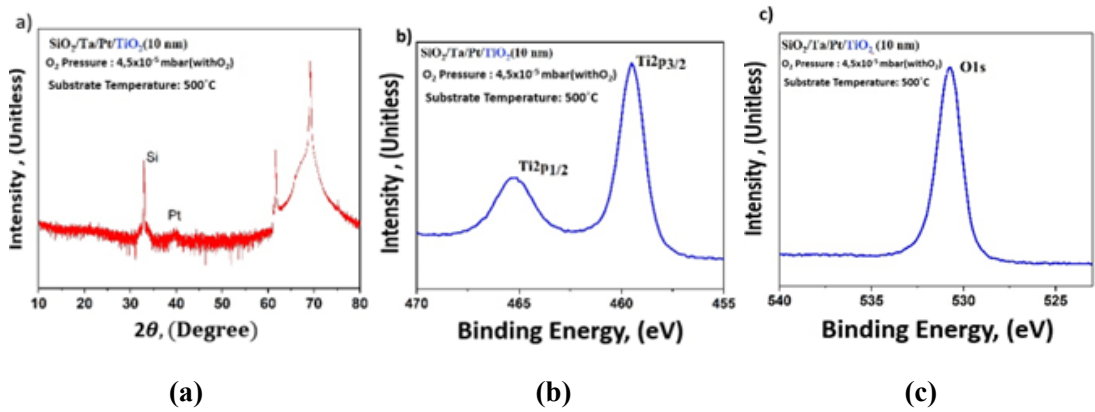


Figure 7.15: a) XRD result of $\text{SiO}_2/\text{Ta}/\text{Pt}/\text{TiO}_2$ thin film, b-c) High-resolution XPS spectra of $\text{Ti}2p$ and $\text{O}1s$.

7.2.3. Structural Characterization of Experiment 2

The experimental results detailing the structural characteristics of TiO_2 were previously presented in Device Fabrication Experiment 1 in Section 7.1. The XRD and XPS results provided in Figure 7.15 specifically indicate that the TiO_2 layer (TiO_x) used in the memristor device structurally contains TiO_2 .

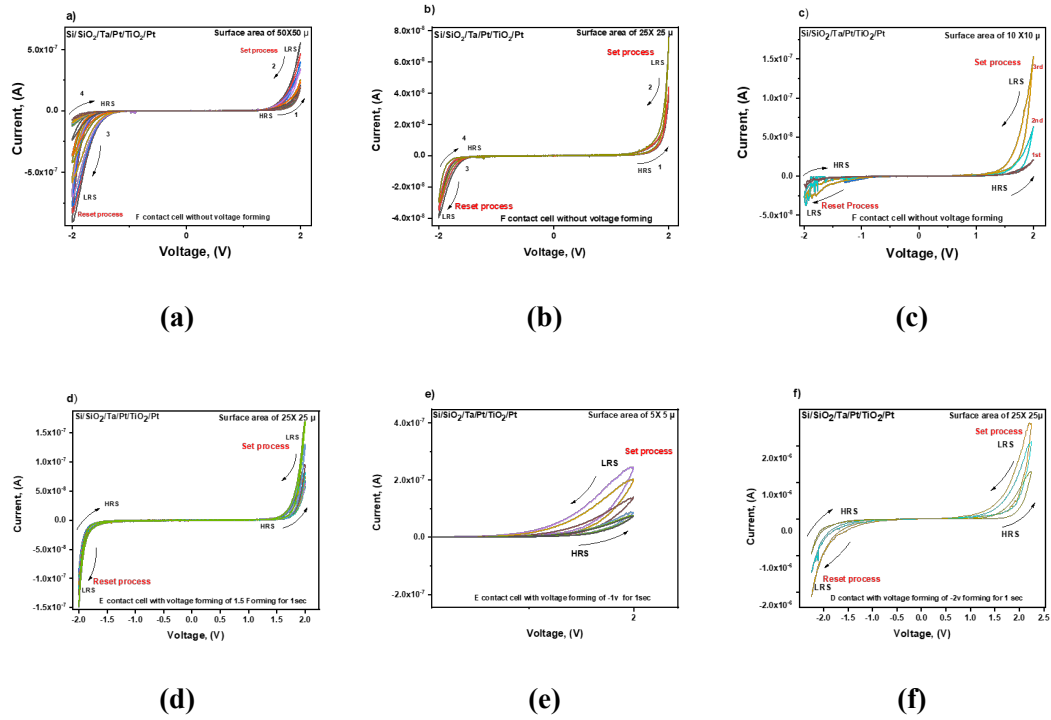


Figure 7.16: The current-voltage characteristics for TiO₂-based memristor devices with different surface areas in different cell contacts position and different voltage forming, a) Memristor device in the F contact cell with 50μ surface area without voltage forming for 50 cycles, b) memristor device in the F contact cell with 25μ surface area without voltage forming, c) memristor device in the F contact cell with 10μ surface area without voltage forming, d) memristor device in the E contact cell with 25μ surface area with forming of (1.5V, 1sec), e) memristor device in the E contact cell with 5μ surface area with forming of (-1V, 1sec), f) memristor device in the D contact cell with 25μ surface area with forming of (-2V, 1sec).

7.2.4. Electrical Characterization of Experiment 2

Instead of experiencing abrupt increases or decreases in current during SET and RESET processes at a high voltage regime, a noteworthy observation is that the device current consistently rises or falls during repeated voltage sweeps, as depicted in Figures 7.16(a-f). When scanned with positive and negative voltages, the gradual increase and decrease in resistance confirm the memristive characteristics of the device. The I-V curve clearly exhibits hysteresis, indicating a transition from RS HRS to LRS for pos-

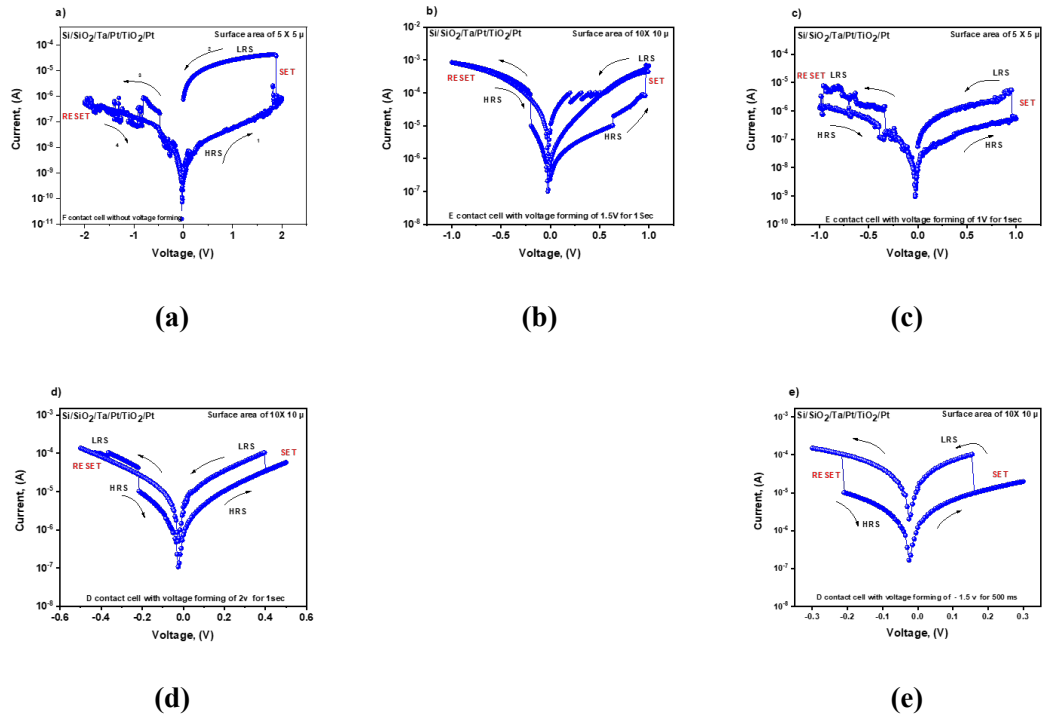


Figure 7.17: The current-voltage characteristics for TiO₂-based memristor devices, a) memristor device in the F contact cell with 5 μ surface area without voltage forming, b) memristor device in the E contact cell with 10 μ surface area with forming of (1.5V, 1sec), c) memristor device in the E contact cell with 5 μ surface area with forming of (1V, 1sec), d) memristor device in the D contact cell with 10 μ surface area with forming of (2V, 1sec), e) memristor device in the D contact cell with 10 μ surface area with forming of (-1.5, 500ms).

itive sweeps and RS from LRS to HRS for negative sweeps. Applying a positive voltage leads to a gradual increase in device conductance, referred to as the write process. Conversely, applying a negative voltage results in a gradual decrease in conductance, known as the erase process. The resistance gradually increases (decreases), revealing multilevel values as the voltage sweeping process is reiterated (Figure 7.16). These graphs show the analog memory characteristics of a neuromorphic device, and these resistive switching (RS) properties may be attributed to the drift of oxygen vacancies, and the progressive rise (or fall) in current throughout positive (or negative) voltage sweeps illustrates the device's capability for resistance modulation in DC-sweeping mode. Additionally, with each successive positive or negative sweep, the I-V curve seamlessly

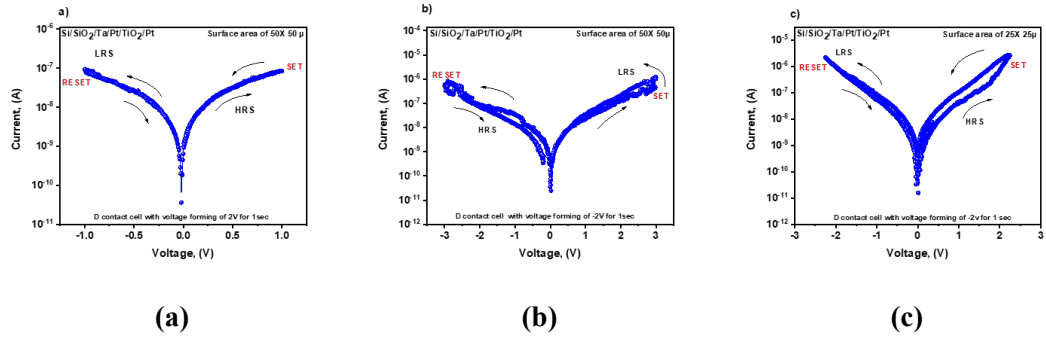


Figure 7.18: The current-voltage characteristics for TiO₂-based memristor devices with low ROFF/RON ratio, a) memristor device in the D contact cell of 50μ surface area with voltage forming (2V, 1sec), b) memristor device in the D contact cell of 50μ surface area with forming of (-2V, 1sec), c) memristor device in the D contact cell of 25μ surface area with forming of (-2V, 1sec).

continues from the previous one, showcasing a characteristic analog switching behavior inherent to memristor devices, as evident in the graphs and this is consistent with the results found in literatures[66–68] .

Furthermore, the characteristic current-voltage curves of memristor devices which show a significantly high ROFF/RON ratio are illustrated in (Figure 7.17). However, in the case of 50 and 25 μ, as depicted in Figure 7.18, a notably low ROFF/RON ratio is achieved. This can be explained by the high surface areas of the devices and the low oxygen vacancy density.

7.2.5. AC Measurement For Synaptic Plasticity of Experiment2

7.2.5.1. Retention Measurement Results

The endurance performance of the memristor device was assessed by testing the retention behaviors at room temperature with a readout voltage of +0.3 V, as illustrated in Figure 7.19. The results indicate that the device can maintain stable and uniform operation between low-resistance state (LRS) and high-resistance state (HRS) during set/reset operations for over 500 cycles. In this context, the LRS and HRS states were programmed using pulsed biases of -2.2 V and 1.5V, respectively, for devices with

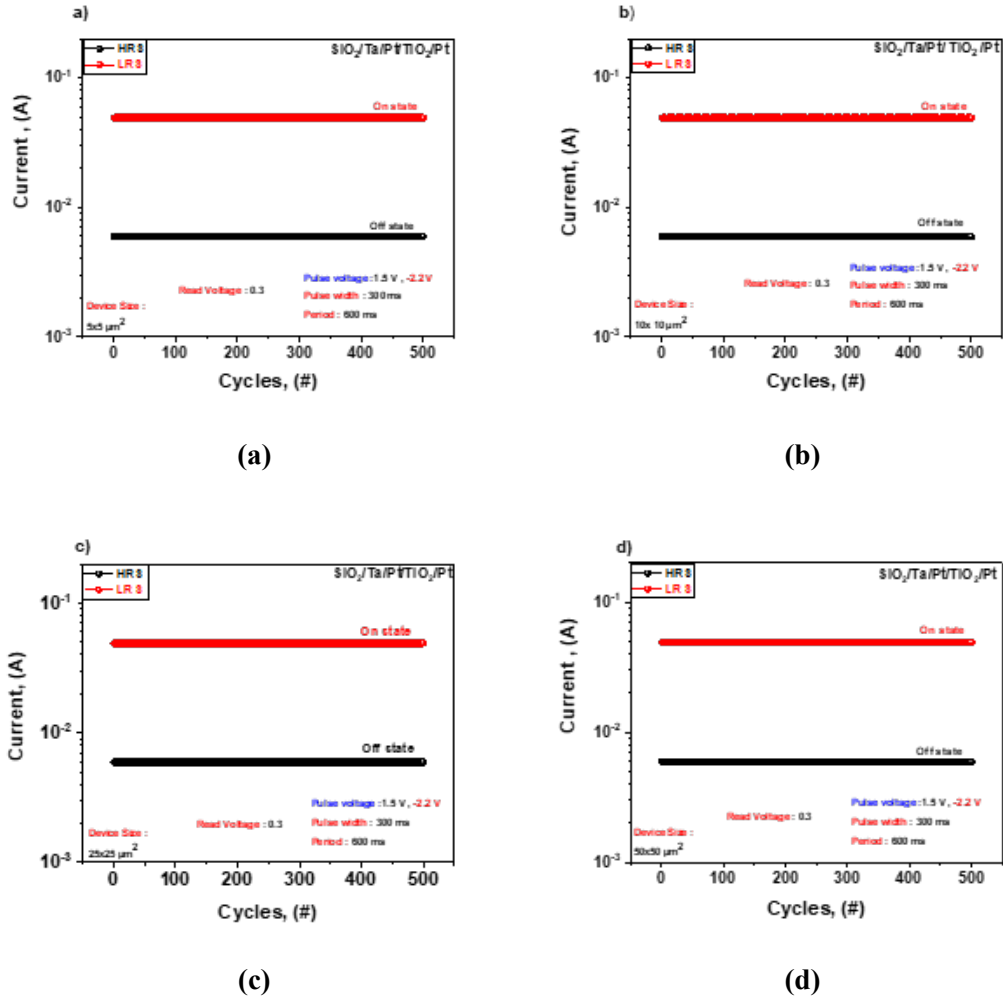


Figure 7.19: Retention characteristics of the memristor devices with different surface areas, a) Memristor device of 5μ Surface area, b) Memristor device of 10μ Surface area, c) Memristor device of 25μ Surface area, d) Memristor device of 50μ Surface area.

varying surface areas (5 , 10 , 25 , 50μ). The pulse widths and periods were consistent at 300 ms and 600 ms, respectively, for all devices. The findings demonstrate that all devices exhibited stable operation throughout 500 cycles, with no significant change in the current levels of the ON (ION) and OFF (IOFF) states.

7.2.5.2. LTP and LTD Measurement Results

Our objective was to emulate potentiation and depression patterns resembling those observed in biological systems by subjecting our memristor devices to successive positive and negative pulses. with surface area structures of $5 \times 5\mu$, $10 \times 10\mu$, and 25

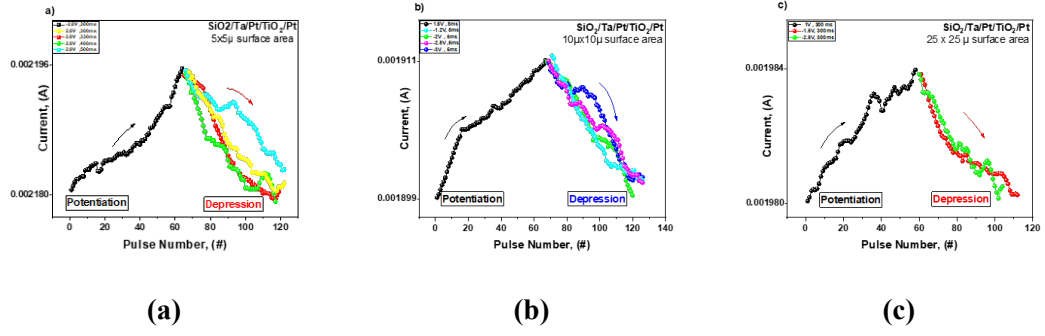


Figure 7.20: Potentiation (60 pulses) and Depression (60 pulses) by applying 120 consecutive pulses in SiO₂/Ta/Pt/TiO₂/Pt devices. Gradual current change of memristor devices a) Memristor device with 5 x 5 μ surface area, b) Memristor device with 10 x 10 μ surface area, c) Memristor device with 15 x 15 μ surface area.

x 25μ. The synaptic performance of our devices is evaluated, as illustrated in Figure 7.20. In our experiments, we employed pulses with different amplitudes to shift from the saturation point of the potentiation response to the depression response, mirroring the behavior seen in biological synapses. The gradual alterations in current, referred to as potentiation and depression induced by successive pulses, align with the mechanisms of Long-Term Potentiation (LTP) and Long-Term Depression (LTD) observed in artificial synapses [69–71]. Furthermore, we observed that the surface area affects these mechanisms of current changes in the devices. The memristor with a smaller surface area of 5 x 5μ exhibits higher current changes, ranging from 0.002180 A to 0.002196 A. However, in the case of devices with larger surface areas of 10 x 10μ and 25 x 25μ, the current change diminishes from 0.001899A to 0.001911 A and from 0.001980 A to 0.001984 A, respectively. We believe that several factors contribute to this observation. One of these factors is that devices with a larger surface area may have longer conduction paths for charge carriers, resulting in increased resistance and slower switching dynamics, ultimately leading to a smaller change in current during the switching process. Additionally, the distribution and concentration of ions or charge carriers involved in the switching process may be more uniform in larger devices, causing reduced concentration gradients and potentially resulting in smaller changes in current compared to devices with smaller surface areas.

8. CONCLUSION

The memristor device we developed underwent comprehensive structural and electrical characterizations, establishing a benchmark for future devices. Our analysis of the oxide layers, specifically TiO₂, revealed a favorable stoichiometric ratio based on XPS results. Analysis of the I-V graphs revealed a uniform pinched hysteresis curve across all devices, a distinctive trait of memristors. Notably, devices with varying oxide layer thickness exhibited distinct set and reset values. Oxygen vacancy levels demonstrated an increasing trend with film thickness from 10 nm to 15 nm. Retention tests validated the enduring and consistent performance of all devices throughout the applied cycles, with negligible changes in current levels between the ON and OFF states. Applying sequential pulses to all devices resulted in incremental current adjustments, mimicking the mechanisms of Long-Term Potentiation (LTP) and Long-Term Depression (LTD) observed in biological synapses. Notably, the achieved modifications in synaptic weight emphasize the potential applicability of these TiO₂-based memristor devices as artificial synapses.

REFERENCES

- [1] Platt C., (2012), “Encyclopedia of Electronic Components Volume 1: Resistors, Capacitors, Inductors, Switches, Encoders, Relays, Transistors”, Vol. 1, ” O’Reilly Media, Inc.”.
- [2] Chua L., (1971), “Memristor-the missing circuit element”, IEEE Transactions on circuit theory, 18(5), 507–519.
- [3] Chua L. O., Kang S. M., (1976), “Memristive devices and systems”, Proceedings of the IEEE, 64(2), 209–223.
- [4] Chua L., (2011), “Resistance switching memories are memristors”, Applied Physics A, 102(4), 765–783.
- [5] Strukov D. B., Snider G. S., Stewart D. R., Williams R. S., (2008), “The missing memristor found”, nature, 453(7191), 80–83.
- [6] Zidan M. A., Omran H., Smith C., Syed A., Radwan A. G., Salama K. N., (2014), “A family of memristor-based reactance-less oscillators”, International Journal of Circuit Theory and Applications, 42(11), 1103–1122.
- [7] Corinto F., Ascoli A., Gilli M., (2012), Modeling dynamics of memristive nanostructures, in “2012 IEEE International Symposium on Circuits and Systems (ISCAS)”, IEEE, 1600–1603.
- [8] Valsa J., Biolek D., Biolek Z., (2011), “An analogue model of the memristor”, International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 24(4), 400–408.
- [9] Benderli S., Wey T., (2009), “On spice macromodelling of TiO₂ memristors”, Electronics letters, 45(7), 1.
- [10] Biolek Z., Biolek D., V B., (2009), “Spice model of memristor with nonlinear dopant drift”, Radioengineering, 18(2), 210–214.
- [11] Kvatinisky S., Friedman E. G., Kolodny A., Weiser U. C., (2012), “Team: Threshold adaptive memristor model”, IEEE transactions on circuits and systems I: regular papers, 60(1), 211–221.
- [12] Batas D., Fiedler H., (2010), “A memristor spice implementation and a new approach for magnetic flux-controlled memristor modeling”, IEEE Transactions on Nanotechnology, 10(2), 250–255.
- [13] Ascoli A., Corinto F., Senger V., Tetzlaff R., (2013), “Memristor model comparison”, IEEE Circuits and Systems Magazine, 13(2), 89–105.
- [14] Abdalla H., Pickett M. D., (2011), Spice modeling of memristors, in “2011 IEEE International Symposium of Circuits and Systems (ISCAS)”, IEEE, 1832–1835.
- [15] Traversa F. L., Pershin Y. V., Di Ventra M., (2013), “Memory models of adaptive behavior”, IEEE transactions on neural networks and learning systems, 24(9), 1437–1448.

- [16] Miao F., Strachan J. P., Yang J. J., Zhang M.-X., Goldfarb I., Torrezan A. C., Eschbach P., Kelley R. D., Medeiros-Ribeiro G., Williams R. S., (2011), "Anatomy of a nanoscale conduction channel reveals the mechanism of a high-performance memristor", *Advanced materials*, 23(47), 5633–5640.
- [17] Elgabra H., Farhat I. A., Al Hosani A. S., Homouz D., Mohammad B., (2012), Mathematical modeling of a memristor device, in "2012 international conference on innovations in information technology (IIT)", IEEE, 156–161.
- [18] Snider G. S., (2008), Spike-timing-dependent learning in memristive nanodevices, in "2008 IEEE international symposium on nanoscale architectures", Ieee, 85–92.
- [19] Yang J. J., Pickett M. D., Li X., Ohlberg D. A., Stewart D. R., Williams R. S., (2008), "Memristive switching mechanism for metal/oxide/metal nanodevices", *Nature nanotechnology*, 3(7), 429–433.
- [20] Pickett M. D., Strukov D. B., Borghetti J. L., Yang J. J., Snider G. S., Stewart D. R., Williams R. S., (2009), "Switching dynamics in titanium dioxide memristive devices", *Journal of Applied Physics*, 106(7), 074508.
- [21] Borghetti J., Strukov D. B., Pickett M. D., Yang J. J., Stewart D. R., Williams R. S., (2009), "Electrical transport and thermometry of electroformed titanium dioxide memristive switches", *Journal of Applied Physics*, 106(12), 124504.
- [22] Miao F., Yang J. J., Strachan J. P., Stewart D., Williams R. S., Lau C. N., (2009), "Force modulation of tunnel gaps in metal oxide memristive nanoswitches", *Applied Physics Letters*, 95(11), 113503.
- [23] Miao F., Ohlberg D., Stewart D. R., Williams R. S., Lau C. N., (2008), "Quantum conductance oscillations in metal/molecule/metal switches at room temperature", *Physical review letters*, 101(1), 016802.
- [24] Strachan J. P., Yang J. J., Münstermann R., Scholl A., Medeiros-Ribeiro G., Stewart D. R., Williams R. S., (2009), "Structural and chemical characterization of tio₂ memristive devices by spatially-resolved nexafs", *Nanotechnology*, 20(48), 485701.
- [25] Yang J. J., Miao F., Pickett M. D., Ohlberg D. A., Stewart D. R., Lau C. N., Williams R. S., (2009), "The mechanism of electroforming of metal oxide memristive switches", *Nanotechnology*, 20(21), 215201.
- [26] Strachan J. P., Strukov D. B., Borghetti J., Yang J. J., Medeiros-Ribeiro G., Williams R. S., (2011), "The switching location of a bipolar memristor: chemical, thermal and structural mapping", *Nanotechnology*, 22(25), 254015.
- [27] Singh J., Raj B., (2019), "An accurate and generic window function for nonlinear memristor models", *Journal of Computational Electronics*, 18, 640–647.
- [28] Simmons J. G., (1963), "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film", *Journal of applied physics*, 34(6), 1793–1803.
- [29] Waser R., Aono M., (2007), "Nanoionics-based resistive switching memories", *Nature materials*, 6(11), 833–840.

- [30] Zhu X.-J., Shang J., Li R.-W., (2012), “Resistive switching effects in oxide sandwiched structures”, *Frontiers of Materials Science*, 6, 183–206.
- [31] Waser R., (2008), Electrochemical and thermochemical memories, in “2008 IEEE International Electron Devices Meeting”, IEEE, 1–4.
- [32] Strukov D. B., Borghetti J. L., Williams R. S., (2009), “Coupled ionic and electronic transport model of thin-film semiconductor memristive behavior”, *Small*, 5(9), 1058–1063.
- [33] Williams R. S., Ribeiro G. M., Strukov D. B., Yang J., (2012), “Controlled switching memristor”, US Patent App. 13/383,597.
- [34] Akinaga H., Shima H., (2010), “Resistive random access memory (reram) based on metal oxides”, *Proceedings of the IEEE*, 98(12), 2237–2251.
- [35] Keshmiri V., (2014), A study of the memristor models and applications, Tech. Rep. LITH-EX-11/4455, Linköping University, Linköping, Sweden.
- [36] Kavehei O., (2011), Memristive devices and circuits for computing, memory, and neuromorphic applications, Technical report, The University of Adelaide, School of Electrical and Electronics Engineering, Adelaide, Australia.
- [37] Hudec B., (2012), “Structures for nanoscale dram memories”, Doktoritöö. Slovak Academy of Sciences, Institute of Electrical Engineering, lk, 14–15.
- [38] Strukov D. B., Williams R. S., (2009), “Exponential ionic drift: fast switching and low volatility of thin-film memristors”, *Applied Physics A*, 94(3), 515–519.
- [39] Kwon D.-H., Kim K. M., Jang J. H., Jeon J. M., Lee M. H., Kim G. H., Li X.-S., Park G.-S., Lee B., Han S., et al. (2010), “Atomic structure of conducting nanofilaments in tio₂ resistive switching memory”, *Nature nanotechnology*, 5(2), 148–153.
- [40] Bashar M. S., Yusoff Y., Abdullah S. F., Rahaman M., Chelvanathan P., Gafur A., Ahmed F., Akhtaruzzaman M., Amin N., (2020), “An investigation on structural and optical properties of zn_{1-x}mg_xs thin films deposited by rf magnetron co-sputtering technique”, *Coatings*, 10(8), 766.
- [41] Limbadri K., James A., (2023), “Optimization of substrate temperature for pulsed laser deposition of SRO”, *Materials Today: Proceedings*.
- [42] Cullity B., Stock S., (2001), “Elements of X-ray Diffraction”, 3rd Edition, Prentice-Hall.
- [43] Kittel C., (2005), “Introduction to solid state physics”, 1st Edition, John Wiley & sons, inc.
- [44] Warren B. E., (1990), “X-ray Diffraction”, 1st Edition, Courier Corporation.
- [45] Özkal B., (2019), Electron paramagnetic resonance studies on oxygen related defects in memristive system, PhD thesis, Gebze Technical University. Accessed: 2010-09-30.
- [46] Kachhadiya D. D., Sonawane A. V., Murthy Z., (2022), Metal–organic frame-

- works (mofs) characterization using different analytical methods, in “Metal-Organic Frameworks (MOFs) as Catalysts”, Springer, 165–180.
- [47] Filies O., Böling O., Grewer K., Lekki J., Lekka M., Stachura Z., Cleff B., (1999), “Surface roughness of thin layers—a comparison of xrr and sfm measurements”, *Applied surface science*, 141(3-4), 357–365.
 - [48] Stevie F. A., Donley C. L., (2020), “Introduction to x-ray photoelectron spectroscopy”, *Journal of Vacuum Science Technology A*, 38(6), 063204.
 - [49] Yakopcic C., (2011), *Memristor Devices: Fabrication, Characterization, Simulation, and Circuit Design*, PhD thesis, University of Dayton.
 - [50] Chua L., (2013), “Memristor, hodgkin–huxley, and edge of chaos”, *Nanotechnology*, 24(38), 383001.
 - [51] Yang N., Zhang J., Huang J.-K., Liu Y., Shi J., Si Q., Yang J., Li S., (2022), “Multitasking memristor for high performance and ultralow power artificial synaptic device application”, *ACS Applied Electronic Materials*, 4(6), 3154–3165.
 - [52] Versace M., Chandler B., (2010), “The brain of a new machine”, *IEEE spectrum*, 47(12), 30–37.
 - [53] Kim K.-H., Gaba S., Wheeler D., Cruz-Albrecht J. M., Hussain T., Srinivasa N., Lu W., (2012), “A functional hybrid memristor crossbar-array/cmos system for data storage and neuromorphic applications”, *Nano letters*, 12(1), 389–395.
 - [54] Chang T., Jo S.-H., Lu W., (2011), “Short-term memory to long-term memory transition in a nanoscale memristor”, *ACS nano*, 5(9), 7669–7676.
 - [55] Yang R., Terabe K., Liu G., Tsuruoka T., Hasegawa T., Gimzewski J. K., Aono M., (2012), “On-demand nanodevice with electrical and neuromorphic multifunction realized by local ion migration”, *ACS nano*, 6(11), 9515–9521.
 - [56] Park J., Park E., Kim S., Yu H.-Y., (2019), “Nitrogen-induced enhancement of synaptic weight reliability in titanium oxide-based resistive artificial synapse and demonstration of the reliability effect on the neuromorphic system”, *ACS applied materials & interfaces*, 11(35), 32178–32185.
 - [57] Wei Z., Kanzawa Y., Arita K., Katoh Y., Kawai K., Muraoka S., Mitani S., Fujii S., Katayama K., Iijima M., et al. (2008), Highly reliable taox reram and direct evidence of redox reaction mechanism, in “2008 IEEE international electron devices meeting”, IEEE, 1–4.
 - [58] Lee M.-J., Lee C. B., Lee D., Lee S. R., Chang M., Hur J. H., Kim Y.-B., Kim C.-J., Seo D. H., Seo S., et al. (2011), “A fast, high-endurance and scalable non-volatile memory device made from asymmetric ta₂o₅- x/tao₂- x bilayer structures”, *Nature materials*, 10(8), 625–630.
 - [59] Govoreanu B., Kar G. S., Chen Y., Paraschiv V., Kubicek S., Fantini A., Radu I., Goux L., Clima S., Degraeve R., et al. (2011), 10× 10nm² hf/hfo x crossbar resistive ram with excellent performance, reliability and low-energy operation, in “2011 International Electron Devices Meeting”, IEEE, 31–6.

- [60] Pi S., Li C., Jiang H., Xia W., Xin H., Yang J. J., Xia Q., (2019), “Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension”, *Nature nanotechnology*, 14(1), 35–39.
- [61] Torrezan A. C., Strachan J. P., Medeiros-Ribeiro G., Williams R. S., (2011), “Sub-nanosecond switching of a tantalum oxide memristor”, *Nanotechnology*, 22(48), 485203.
- [62] Sung J. H., Park J. H., Jeon D. S., Kim D., Yu M. J., Khot A. C., Dongale T. D., Kim T. G., (2021), “Retention enhancement through capacitance-dependent voltage division analysis in 3d stackable ta₂O₅/hfo₂-based selectorless memristor”, *Materials & Design*, 207, 109845.
- [63] Jang J.-W., Park S., Burr G. W., Hwang H., Jeong Y.-H., (2015), “Optimization of conductance change in pr 1–x ca x mno 3-based synaptic devices for neuromorphic systems”, *IEEE Electron Device Letters*, 36(5), 457–459.
- [64] Wang I.-T., Chang C.-C., Chiu L.-W., Chou T., Hou T.-H., (2016), “3D Ta/TaO_x/TiO₂/Ti synaptic array and linearity tuning of weight update for hardware neural network applications”, *Nanotechnology*, 27(36), 365204.
- [65] Tanim M. M. H., Templin Z., Zhao F., (2023), “Natural organic materials based memristors and transistors for artificial synaptic devices in sustainable neuromorphic computing systems”, *Micromachines*, 14(2), 235.
- [66] Nagata Z., Shimizu T., Isaka T., Tohei T., Ikarashi N., Sakai A., (2019), “Gate tuning of synaptic functions based on oxygen vacancy distribution control in four-terminal tio₂- x memristive devices”, *Scientific Reports*, 9(1), 10013.
- [67] Lee D.-H., Park H., Cho W.-J., (2023), “Implementation of highly stable memristive characteristics in an organic–inorganic hybrid resistive switching layer of chitosan-titanium oxide with microwave-assisted oxidation”, *Molecules*, 28(13), 5174.
- [68] Xiao M., (2019), One-dimensional Titanium Dioxide Nanomaterial based Memristive Device and its Neuromorphic Computing Applications, PhD thesis, University of Waterloo. PhD thesis, UWSpace.
- [69] Guo J., Liu L., Bian B., Wang J., Zhao X., Zhang Y., Yan Y., (2023), “Ligand exchange reaction enables digital-to-analog resistive switching and artificial synapse within metal nanoparticles”, *Advanced Functional Materials*, 33(16), 2212666.
- [70] Wu Y., Huang H., Xu C., Cao X., Lei Z., Zhang J., Zhao Y., Wei A., Liu Z., (2023), “The fapbi₃ perovskite memristor with a pmma passivation layer as an artificial synapse”, *Applied Physics A*, 129(5), 1–8.
- [71] Subin P., Asha A., Saji K., Jayaraj M., (2021), “Spike-dependent plasticity modulation in tio₂-based synaptic device”, *Journal of Materials Science: Materials in Electronics*, 32(10), 13051–13061.

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2. Ekinici, G., Özkal, B., Al-Jawfi, N. A. A., Kazan, S. (2023). Investigation of Optical and Structural Properties of VO₂ Thin Films by Thermal Treatment. *Journal of Advanced Applied Sciences*, 2(2), 57-63.
3. Tokaç, M., Kazan, S., Özkal, B., Al-jawfi, N., Rameev, B., Nicholson, B., Hindmarch, A. T. (2023). Two Magnon Scattering Contribution to the Ferromagnetic Resonance Linewidth of Pt (Ir)/CoFeTaB/Ir (Pt) Thin Films. *Applied Magnetic Resonance*, 54(10), 1053-1064.