

T.R.
GEBZE TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

SWITCHED-CAPACITOR CIRCUITS AND APPLICATIONS

İRFAN YAKUT
A THESIS SUBMITTED FOR THE DEGREE OF
MASTER OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

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GEBZE TEKNİK ÜNİVERSİTESİ
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SWITCHED-CAPACITOR DEVRELERİ
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SUMMARY

Considering the modern technology trends, significance of the structures which are versatile and compliant of semiconductor integrated circuit manufacturing processes can be understood. In this context, Switched-Capacitor Circuits and Applications are studied in this thesis, which are one of the most important structure developed in order to satisfy the demand mentioned above.

In first chapter, the reason why MOSFET switches has chosen in order to implement switch function in Switched-Capacitor Circuits, their advantages and disadvantages comparing to their counterparts, their physical structure, their characteristic curves and how they can be used as switches are explained. At the end of this chapter, NMOS and PMOS spice models' characteristics, which are used in the applications presented in the third chapter, are presented.

In second chapter, requirements necessary in order to use NMOS and PMOS as switches, their performances as switches and passing characteristics are presented. Afterwards, Transmission Gates introduced. The structure of these switches and reason of their superior performance comparing to the NMOS and PMOS are explained.

In third chapter, analyses, test circuits and simulation result of Simulated Resistor, First-Order Low-Pass Filter and Common-Mode Feedback Circuits, which are comprise of the Switched-Capacitor circuits are presented.

Simulations presented in this thesis have made by using LTspice® and ngspice SPICE simulation tools. Also, MOSFET models used in simulations are the "45nm High-Performance Predictive Technology Model" spice models created by NIMO Group at Arizona State University (ASU) according to criteria created by The BSIM Group.

Key Words: MOSFET Switch, Switched-Capacitor, Low-Pass Filter, Integrator, Common-Mode Feedback.

ÖZET

Günümüzde teknolojinin takip ettiği trend göz önüne alınacak olursa yarıiletken tümdevre üretim süreçlerine uygun ve esnek yapıların önemi anlaşılmaktadır. Bu bağlamda, bu tez çalışmasında bu yapıların başında gelen Anahtarlama-Kapasite Devreleri ve Uygulamaları incelenmiştir.

İlk bölümde, Anahtarlama-Kapasite Devrelerini oluştururken anahtar olarak neden MOSFET anahtarların seçildiği, muadillerine kıyasla avantajlı ve dezavantajı oldukları noktalar, fiziksel yapısı, karakteristik eğrileri ve anahtar olarak çalışmaları için nasıl kullanılmaları gerektiği açıklanmıştır. Bu bölümün sonunda, son bölümdeki uygulamalarda kullanılacak olan NMOS ve PMOS spice modellerinin karakteristikleri gösterilmiştir.

İkinci bölümde, NMOS ve PMOS'un anahtar olarak kullanılabilmesi için sağlanması gereken şartlar, anahtar olarak gösterdikleri performanslar ve geçiş karakteristikleri sunulmuştur. Daha sonra İletim Kapısı yapısı tanıtılmıştır. Bu yapının nasıl oluşturulduğu, anahtar olarak kullanıldığında neden NMOS veya PMOS'a kıyasla daha iyi bir performans gösterdiği ve karakteristiği açıklanmıştır.

Son olarak Anahtarlama-Kapasite yapısı kullanılarak oluşturulmuş olan Simüle Direnç, Birinci Mertebe Alçak-Geçiren Filtre ve Ortak-Mod Geri Besleme devrelerinin analizleri, test devreleri ve simülasyon sonuçları paylaşılmıştır. Bu tez çalışmasında yapılan simülasyonlar LTspice® ve ngspice yazılımları kullanılarak yapılmıştır. Ayrıca kullanılan MOSFET modelleri, Arizona Eyalet Üniversitesi (ASU) bünyesindeki Nano Ölçekli Entegrasyon ve Modelleme (NIMO) Grubu tarafından geliştirilmiş olan “45nm High-Performance Predictive Technology Model” spice modelidir. Bu model, Berkeley Kısa-kanal IGFET Model (BSIM) kriterleri doğrultusunda geliştirilmiş modellerdir.

Anahtar Kelimeler: MOSFET Anahtar, Anahtarlama-Kapasite, Alçak-Geçiren Filtre, Integral Alıcı, Ortak-Mod Geri Besleme.

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LIST of ABBREVIATIONS and ACRONYMS

<u>Abbreviations and Acronyms</u>	<u>Explanations</u>
μ_n	: Electron mobility on the channel surface
ω_0	: Characteristic frequency
C_{GD}	: Gate-Drain capacitance of MOSFET
C_{GS}	: Gate-Source capacitance of MOSFET
C_{ox}	: Oxide capacitance or Gate capacitance per unit gate area
f_{CLK}	: Clock or switching frequency of the Switched-Capacitor
f_c	: Cut-Off or Corner frequency
f_{source}	: Frequency of the source voltage
$H(j\omega)$	: Transfer function
I_D	: Drain current
I_G	: Gate current
I_S	: Source current
I_{avg}	: Average current
L	: Length of the channel
L_{min}	: Minimum channel length
$q(t)$	: Charge on C at time t
$q_L(t)$	: Charge on C_L at time t
$q_L(t - T_{CLK})$	: Charge left from the last cycle, computed at $(t - T_{CLK})$
r_{DSOFF}	: Drain-Source resistance when MOSFET is in OFF state
$r_{DSOn_{eq}}$	: Equivalent Drain-Source resistance of Transmission Gate
r_{DSOn}	: Drain-Source resistance when MOSFET is in ON state
R_{eq}	: Equivalent Switched-Capacitor resistor
SiO_2	: Silicon Dioxide
T_{CLK}	: Clock or switching period of the Switched-Capacitor
t_{ox}	: Thickness of the SiO_2 Layer
V_{DS}	: Drain-Source voltage

V_{eff}	:	Effective voltage
V_{GD}	:	Gate-Drain voltage
V_{GS}	:	Gate-Source voltage
V_{icm}	:	Input Common-Voltage
V_{id}	:	Voltage difference between input terminals
V_{ocm}	:	Output Common-Voltage
V_{od}	:	Voltage difference between output terminals
V_{ov}	:	Overdrive voltage
V_{SB}	:	Source-Bulk voltage
V_{SD}	:	Source-Drain voltage
V_{th_N}	:	NMOS's threshold voltage
V_{th_P}	:	PMOS's threshold voltage
V_{th}	:	Threshold voltage
W	:	Width of the channel
W_{NMOS}	:	NMOS's Channel width
W_{PMOS}	:	PMOS's Channel width
ADC	:	Analog to Digital Converter
ASU	:	Arizona State University
BJT	:	Bipolar Junction Transistor
$BSIM$	:	Berkeley Short-Channel IGFET Model Group
$CMFB$	:	Common-Mode Feedback
$CMOS$	:	Complementary Metal-Oxide-Semiconductor
DC	:	Direct Current
$EECS$	:	Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley
FDA	:	Fully-Differential Amplifier
FET	:	Field-Effect Transistor
IC	:	Integrated Circuit
$IGFET$	:	Insulated Gate FET
KCL	:	Kirchhoff's Current Law
$MOSFET$	:	Metal-Oxide-Semiconductor Field-Effect Transistor
$NIMO$	:	Nanoscale Integration and Modeling Group
$NMOS$	:	N-Channel MOSFET

<i>Op – Amp</i>	:	Operational Amplifier
<i>PMOS</i>	:	P-Channel MOSFET
<i>PTM</i>	:	Predictive Technology Model
<i>SC</i>	:	Switched-Capacitor
<i>SPST</i>	:	Single-Pole Single-Throw
<i>TG</i>	:	Transmission Gate
<i>VLSI</i>	:	Very Large-Scaled Integrated

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1. INTRODUCTION

The origins of the electronics industry date back to the late 1800s. Since then, thanks to the studies carried out both in terms of design and production, great progress has been achieved in this field of application. Nowadays, it is possible to produce semiconductor transistors of 7nm in size and this technological improvement made it possible to fit millions of transistors into a single integrated circuit.

At this point, it has become possible to perform much more complex processes with much faster and less energy consumption, but the advancement of technology forces scientists and engineers to find creative solutions to produce better technologies.

Switched-Capacitor circuits discussed in this thesis are one of the solutions found in line with this motivation. The basic principles of the Switched-Capacitor structure were laid down by James Clerk Maxwell in the late 1800s, and the first theoretical studies on this topic were introduced in the 1970s and numerous studies and applications have been made on this subject since then. The Switched-Capacitor structure allows for the creation of programmable and small structures consisting entirely of transistors, rather than components such as resistor and capacitor which occupy large area in ICs and have low accuracy. Because of these features, the Switched-Capacitor structure is a promising structure that is suitable for modern production and design processes and is still an active field of study.

The aim of this thesis is to create an understanding of Switched-Capacitor structure and to provide a good understanding of this concept. In this context, the components that make up the Switched-Capacitor circuits are introduced first. The characteristic properties of these components are theoretically expressed and the results obtained are supported by simulation outputs. Then, applications which were created by using Switched-Capacitor structure were examined in detail.

The detailed investigations, theoretical studies, simulations and applications presented in this thesis form a good basis with regard to Switched-Capacitor structure. For this reason, it is highly probable that this thesis will be used as a resource in many future studies. In this respect, it is possible to foresee that this study will contribute to the literature.

2. FUNDAMENTALS of METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

2.1. Introduction

This chapter focuses on explaining the fundamentals of Metal-Oxide-Semiconductor Field-Effect Transistor's (MOSFET's) physical structure and operation. Information presented in this chapter is considered important since it provides a basis for subsequent chapters. To this end, after some background information about MOSFET, some further explanation about MOSFET types, their physical structure and operation will be presented.

2.2. History of MOSFET

Julius Edgar Lilienfeld has laid the foundations for Field-Effect Transistor in 1925 [9]. After Lilienfeld's conceptual studies, some other scientists such as Oskar Heil[6], William Shockley[14] and Dawon Kahng[8] have contributed to this subject with various studies and patents. Although theoretical studies and early laboratory works of FETs have been carried out at the late 1920s, the first properly working prototype has been produced at 1950s. But being lacking of the necessary production technologies and production methods, it had took one more decade for scientists to create necessary production technologies and release the first batch of MOSFETs to the market. Since 1960s, popularity of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has been increasing day by day.[15],[16]

2.3. MOSFET-BJT Comparison

Another semiconductor transistor type, which have been invented approximately two decades after MOSFET's invention and became very popular in a short period of time, is Bipolar Junction Transistor (BJT)[17],[14]. Over the years, due to technolo-

gical improvements in both design and manufacturing of semiconductors, MOSFET's popularity has increased and dominated the industry. Nowadays, MOSFET is the most preferred semiconductor switch for designers because of its various advantages over BJT.[18]

Comparing to BJT, MOSFET can be produced in smaller sizes. Thus, MOSFET takes up smaller place in an integrated circuit (IC). Capability to work with smaller powers, having relatively less complicated manufacturing processes and using smaller control currents have made MOSFET a better choice over BJT. MOSFET's size has been becoming smaller and smaller every year since its invention because of the technological advances. In present day conditions, it is possible to manufacture a VLSI (Very Large-Scaled Integrated) circuit consisting of millions of 7nm MOSFETs.[13]

2.4. Physical Structure of MOSFET

The most commonly used type of MOSFET is the *Enhancement-Type MOSFET*. Therefore, explanations, analyses and simulations which is going to be presented in the rest of this study will be based on N-Channel and P-Channel Enhancement-Type MOSFETs.

2.4.1. Physical Structure of NMOS

As presented in Figure 2.1, an N-Channel MOSFET (NMOS) basically composes of two heavily doped n-type region placed in a p-type substrate. By placing two metal contacts on top of the n-type regions, terminals called as Drain (D) and Source (S) have been obtained. By placing a Silicon Dioxide (SiO_2) layer with thickness of t_{ox} between Drain and Source terminals and a metal contact on top of SiO_2 layer, Gate (G) terminal have been obtained. Also, placing a metal contact under the p-type substrate, terminal called Bulk or Body (B) have been obtained. This structure is the reason why it is called *Metal-Oxide-Semiconductor*. Although, methods and materials have been changed over the time as a consequence of the technological advances, the main principal has been stayed same.

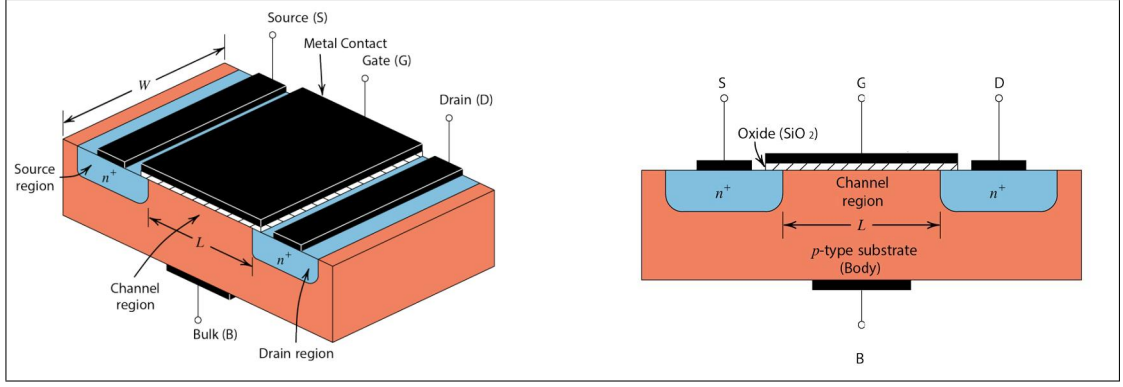


Figure 2.1: Physical structure of NMOS.

As mentioned earlier, there is a SiO_2 insulation layer exists between the Gate terminal and substrate of the MOSFET. Because of this structure, the terms MOSFET and *IGFET (Insulated-Gate Field-Effect Transistor)* can be used interchangeably. Because of this insulation layer, Gate current (I_G) becomes very small and it is an important parameter which contributes to MOSFETs popularity.

As it can be seen on Figure 2.1, there are two pn junctions between p-type substrate and n-type regions. These junctions, in effect, behave like diodes. These two diodes' anode terminal is mutual and it consists of p-type substrate. Obviously, at the time when potential of the Bulk terminal of the NMOS become higher than Drain or Source terminals, these virtual diodes conduct current. Under normal operating conditions, NMOS only conducts current from Drain to Source, so Source must have a lower potential than both Gate and Drain terminals. In order to ensure that, these two pn-junctions must be kept reverse biased all the time. The easiest way to accomplish that is to connect Bulk to the Source. By doing this, it can be guaranteed that there won't be any current flow from Bulk to other terminals and the Source and the Bulk will be kept at the lowest potential among all the terminals. Connecting Bulk terminal to the lowest potential in the *circuit* to keep these two diodes reverse biased under any circumstance is another way to guarantee that which is a very popular common practice used in IC design. Therefore, in the simulations within the scope of this study, latter method has preferred.

However this configuration may introduce a new issue called "*Body Effect*" which needs to be handled carefully. However this effect will be neglected in this study.

2.4.2. Physical Structure of PMOS

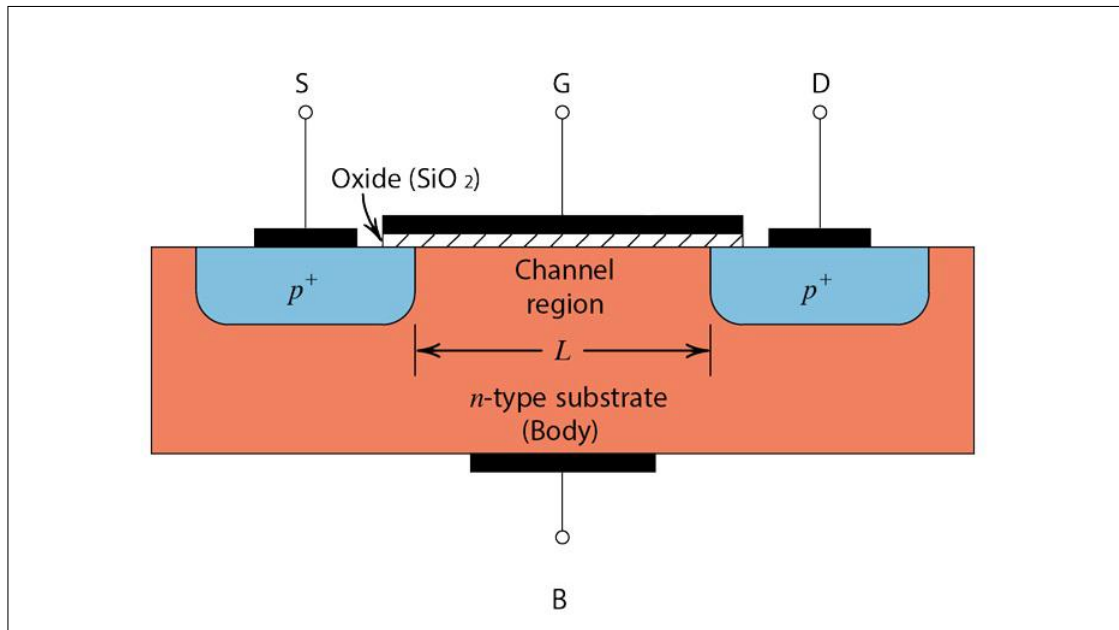


Figure 2.2: Physical structure of PMOS.

At Figure 2.2, physical structure of a P-Channel MOSFET (PMOS) is presented. PMOS's physical structure shows a big resemblance with NMOS's. However, as it can be seen in Figure 2.2, type of the regions in PMOS are different. In other words, PMOS's Drain and Source regions consist of p-type heavily doped material and PMOS's Body consists of n-type substrate. Thus, compared to NMOS, PMOS operates in a complementary fashion. Because of this difference, polarization of PMOS's terminals have to be the exact opposite of the NMOS's. That is to say, under normal operating conditions, PMOS only conducts current from Source to Drain, so Drain must have a lower potential than both Gate and Source terminals. In just the same way with NMOS, PMOS has two pn junctions which behave like diodes either. As it explained earlier, these diodes should be kept reverse biased and in order to ensure that Bulk terminal must be connected to the highest potential in the circuit.

2.5. Operation of MOSFET

This study is focused on MOSFETs switch function. Thus, in this context, MOSFETs' operation in Cut-Off and Triode Regions will be analyzed and explained in detail. However detailed analyses about MOSFETs' operation in Saturation Region will be excluded.

2.5.1. Operation of NMOS

In an NMOS, in order to establish a current flow from Drain to Source, first, a channel must be created in p-type substrate between Drain and Source regions as presented in Figure 2.3. This area has been named as '*Channel*' because its function is same as a water channel, they both let current flow through them. Since the channel region is comprised of n-type material, this MOSFET is called *N-Channel MOSFET* or *NMOS*.

In literature, since an applied v_{GS} changes p-type substrate into n-type, the term '*Inversion Layer*' is used as synonym of '*Channel*'. Another synonym used to define this region is *Accumulation Region* because when a negative Gate voltage applied, positive carriers (holes) accumulates in this region. In order to create a channel, a positive voltage must be applied to Gate. More precisely, voltage difference between Gate and Source (v_{GS}) must be positive.

In the setup presented in Figure 2.3, both Drain and Source are connected to the ground and a positive v_{GS} applied. Thus, a channel has created. In order to establish a current flow, after creating a channel, a positive Drain-Source voltage must be applied. Details about the Drain current (i_D) will be explained after some further explanation about MOSFET's operation.

When a positive v_{GS} applied, positive charge accumulates on the metal contact of the Gate terminal, negative charge accumulates in the channel area and free holes in the channel is pushed into the p-type substrate away from the channel area. Thus, the area which was formerly occupied by the free holes become depleted in terms of free holes. This is the reason why this area called the *Depletion Region*.

MOSFET's Gate terminal, channel and insulated layer between them constitute a parallel plate capacitor in effect. As positive charges accumulate on the Gate, negative

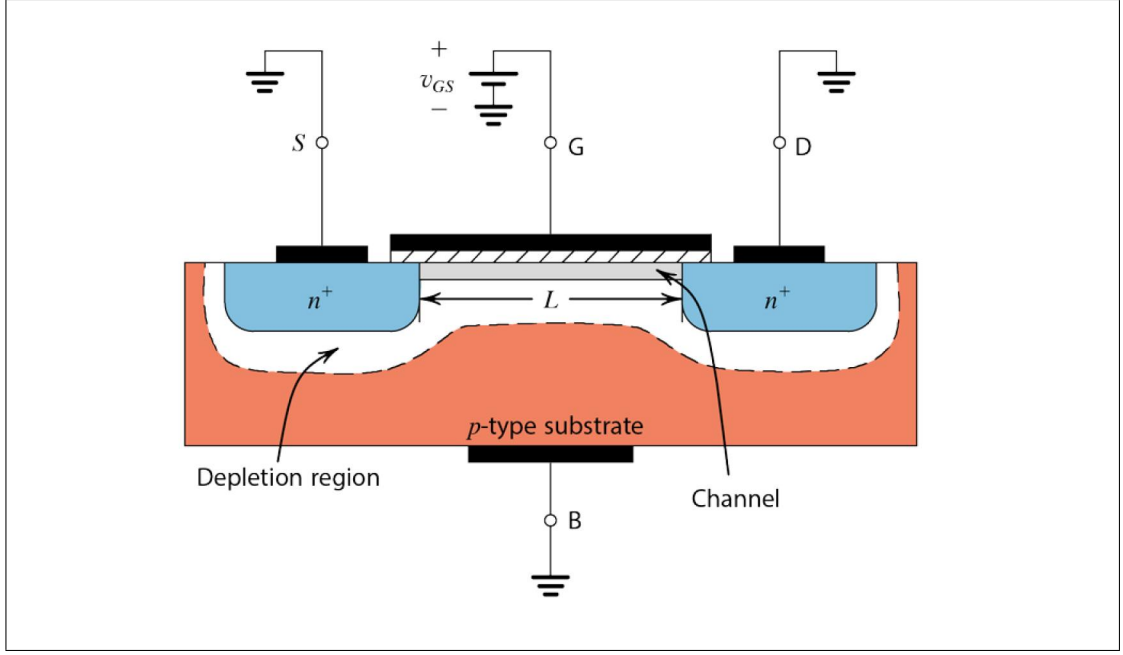


Figure 2.3: Creating a 'Channel' in an Enhancement-Type NMOS applying a positive v_{DS} to Gate terminal.

charges accumulate in the channel and this situation causes to an *Electric Field* occur, which is perpendicular to these layers. Magnitude of this electric field controls the magnitude of the current that flows through the channel. This is the reason why these devices is called as *Field-Effect Transistors*.

In ideal, it is assumed that SiO_2 insulation layer prevents any leakage to other parts of the MOSFET from Gate. But in reality, when a time varying signal applied to the Gate, some charge accumulates in the parallel plate capacitor which is in between the Gate and the Body. In addition to that, C_{GD} and C_{GS} parasitic capacitors cause more leakage. Total impact of these capacitors on leakage is an important issue which needs to be taken into account while a design process. This phenomenon is called *Clock Feedthrough*. On the other hand, after the MOSFET has turned off, residual charge remained in the channel disperses through Drain and Source terminals to the other parts of the circuit. This is another phenomenon to be taken care of and it is called *Charge Injection*. [10],[13]

There are several techniques to minimize or completely remove effects such as Charge Injection or Clock Feedthrough such as dummy switches. However in order to stay on course and not to drift away to aim of this study, these effects will be ignored.

As mentioned earlier, in order to create a channel, a positive v_{GS} must be applied between Gate and Source. Minimum v_{GS} value to create a channel between Drain and Source is called *Threshold Voltage* (V_{th}). Threshold voltage's value should be positive for NMOS ($V_{th_N} > 0$) and negative for PMOS ($V_{th_P} < 0$) and to create a channel following equations must be satisfied:

$$v_{GS} > V_{th_N} \quad (2.1)$$

By satisfying $v_{GS} > V_{th_N}$, channel become *enhanced* and this is the origin of the *Enhancement-Type MOSFET* term. The difference between v_{GS} and V_{th} is called *Effective Voltage* or *Overdrive Voltage*:

$$v_{GS} - V_{th_N} = V_{eff} = V_{ov} \quad (2.2)$$

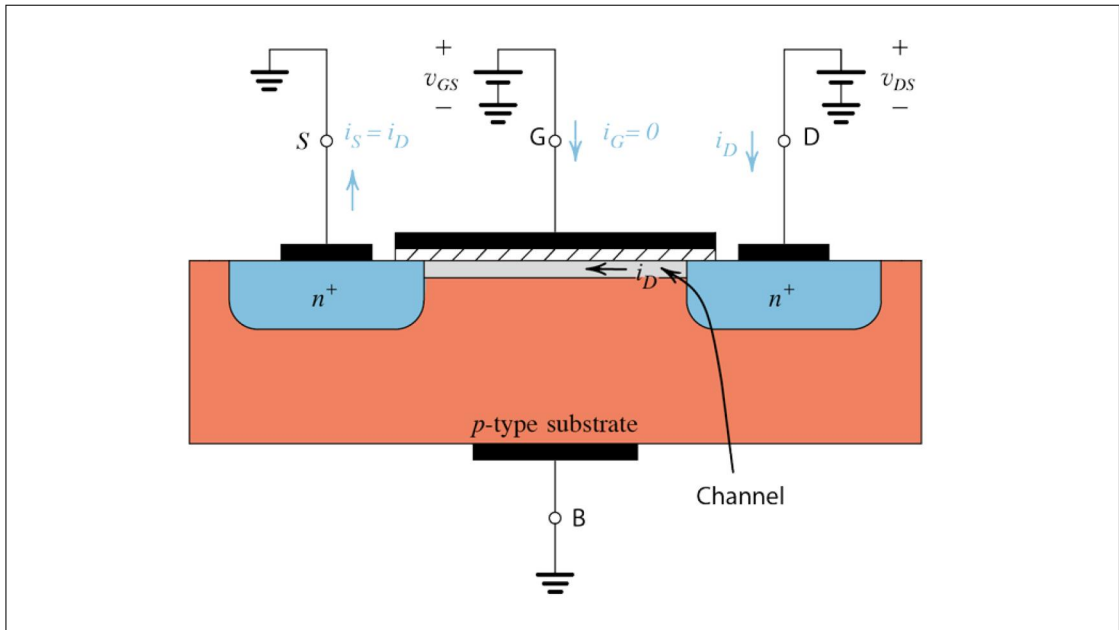


Figure 2.4: Starting current flow through the channel with applying a small positive v_{DS} to Drain terminal.

Once the channel created, by applying a small positive v_{DS} to Drain of the NMOS, a small i_D current is obtained which flows through the channel from Drain to Source as presented in Figure 2.4. The Drain current is carried by the electrons which are majority

carriers in this region. i_D flows from Drain to Source while electrons move the other way around and this operation is the origin of the 'Source' and 'Drain' denominators.

Magnitude of the v_{DS} applied here can be defined as big enough to keep the channel conductive and small enough to protect uniform shape of the channel (same as zero v_{DS} condition). This can be achieved by satisfying $0.1V < v_{DS} \ll V_{eff}$ relationship. This operating region is called *Weak Inversion Region*. While MOSFET is working in this region, i_D increases in direct proportion to v_{DS} till some point, and for a small v_{DS} it can be described with this equation[10],[13]:

$$i_D = \mu_n C_{ox} \left(\frac{W}{L} \right) V_{eff} v_{DS} \quad (2.3)$$

When $v_{DS} < 0.1V$ MOSFET is said to be working in *Subthreshold Region*. [10],[13]

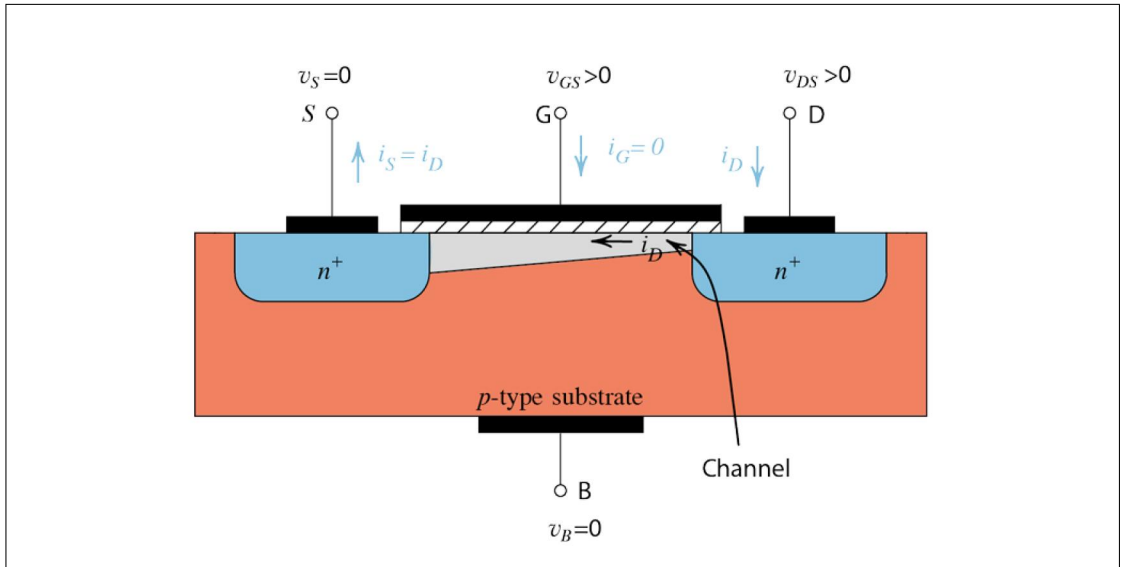


Figure 2.5: Observing the change in the shape of the channel with applying a bigger positive v_{DS} to Drain terminal.

In a channel, which has a uniform shape, potential difference between Gate and a point in the channel does not change throughout the channel and is equal to v_{eff} . Depth of the channel is directly proportionate to magnitude of v_{DS} . When a sufficiently large v_{DS} is applied, which is in the range of $0.5V_{eff} < v_{DS} < V_{eff}$, the channel doesn't keep its uniform shape and the voltage across the channel varies. As presented in Figure 2.5, channel's deepest point is the Source end and the most shallow point is the Drain end.

Clearly, the channel's shape becomes more conical as v_{DS} increases and resistance of the channel increases proportionally. Also, measured voltage on channel changes from Drain to Source between $0V$ and v_{DS} . Voltage difference between Gate and the channel also changes from Drain to Source between v_{GS} and v_{GD} and these two voltages can be expressed with following equations[10],[13]:

$$v_{GS} = V_{th_N} + V_{eff} \quad (2.4)$$

$$v_{GD} = v_{GS} - v_{DS} = V_{th_N} + V_{eff} - v_{DS} \quad (2.5)$$

In the light of these, it is safe to say that there is a direct proportion between the charge accumulated in the channel and the channel's cross-sectional area. For the v_{DS} value in the range of $0 < v_{DS} < V_{eff}$, V_{eff} replaced with the $(V_{eff} - \frac{v_{DS}}{2})$ in the equation (2.3) and new equations becomes this[10]:

$$i_D = \mu_n C_{ox} \left(\frac{W}{L} \right) \left(V_{eff} - \frac{v_{DS}}{2} \right) v_{DS} \quad (2.6)$$

As mentioned earlier, channel resistance increases with v_{DS} and follows a linear line when v_{DS} is small enough to keep channel's shape uniform. In this voltage range, channel resistance increase ratio is very small comparing to the v_{DS} . However, at the point of v_{DS} increased to a voltage level where the channel starts to become conical, its resistance's increase ratio overtakes v_{DS} 's increase ratio and $i_D - v_{DS}$ curve starts to bend as it is presented in Figure 2.6.

This operating mode, where v_{DS} is in the range of $0 < v_{DS} \leq V_{eff}$, is called **Triode Region** or **Linear Region**. When MOSFET is working in Triode Region, the channel depth in the Drain end is bigger than zero in despite of the channel has conical shape. This behaviour continues until v_{DS} reaches V_{eff} .

After that point, for v_{DS} values bigger than V_{eff} , MOSFET goes into another operating mode called **Saturation Region** or **Active Region**. In Saturation Region $v_{DS} \geq V_{eff}$ and $v_{GD} \leq V_{th}$ and channel depth in the Drain end becomes zero and this situation is called *Channel Pinch-Off*.

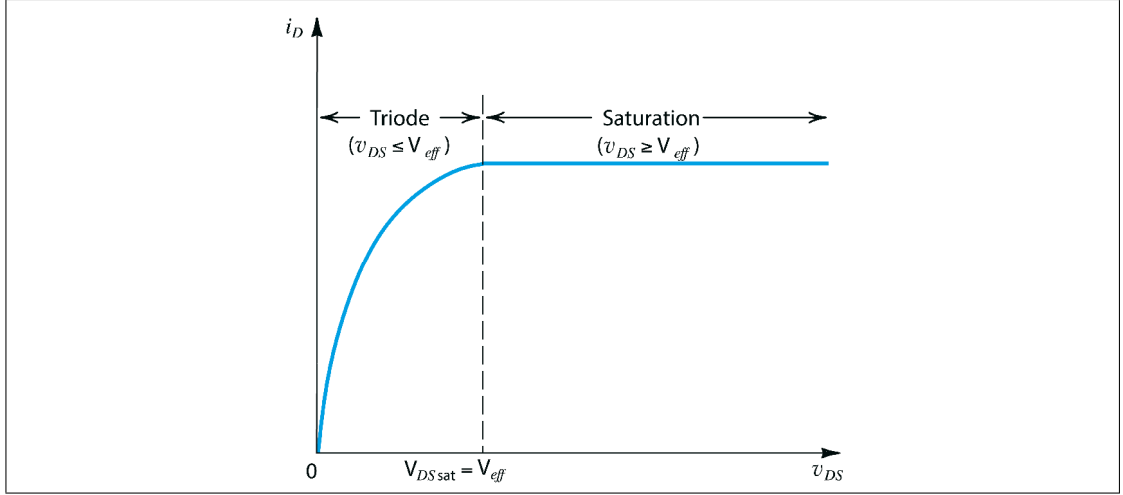


Figure 2.6: $i_D - v_{DS}$ characteristic curve for NMOS.

As presented in Figure 2.6, $v_{DS} = V_{eff}$ is the boundary point between Triode and Saturation Regions. Between $v_{DS} = 0V$ and $v_{DS} = V_{eff}$, NMOS's $i_D - v_{DS}$ curve changes in compliance with the function given in equation 2.6. At the moment v_{DS} reaches V_{eff} , equation 2.6 becomes this:

$$\begin{aligned}
 i_D &= \mu_n C_{ox} \left(\frac{W}{L} \right) \left(V_{eff} - \frac{v_{DS}}{2} \right) v_{DS} \\
 &= \mu_n C_{ox} \left(\frac{W}{L} \right) \left(V_{eff} - \frac{V_{eff}}{2} \right) V_{eff} \\
 &= \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{eff})^2
 \end{aligned} \tag{2.7}$$

As it can be seen on equation 2.7, channel becomes pinched-off after $v_{DS} = V_{eff}$ situation. After that point any further increase on v_{DS} does not effect i_D and it remains constant. Because of this behaviour, i_D defined as saturated.

It should be noted that analysis of $i_D - v_{DS}$ curve mentioned above is based on some assumptions about the operation of NMOS and some body and channel effects are ignored. Therefore, this behaviour of the NMOS's $i_D - v_{DS}$ curve which presented in Figure 2.6 does not coincide with the real behaviour. Cause of this difference is the phenomenon called *Channel Length Modulation* and is presented in Figure 2.7. However, since the scope of this study will be limited with Triode and Cut-off Operation Regions this phenomenon won't further analyzed.

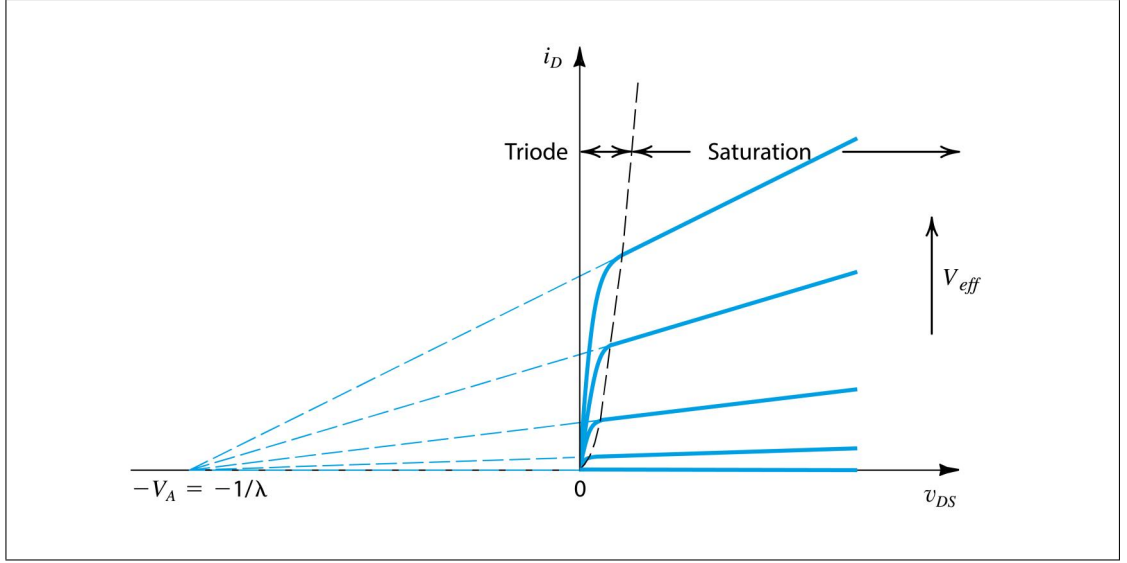


Figure 2.7: Channel Length Modulation

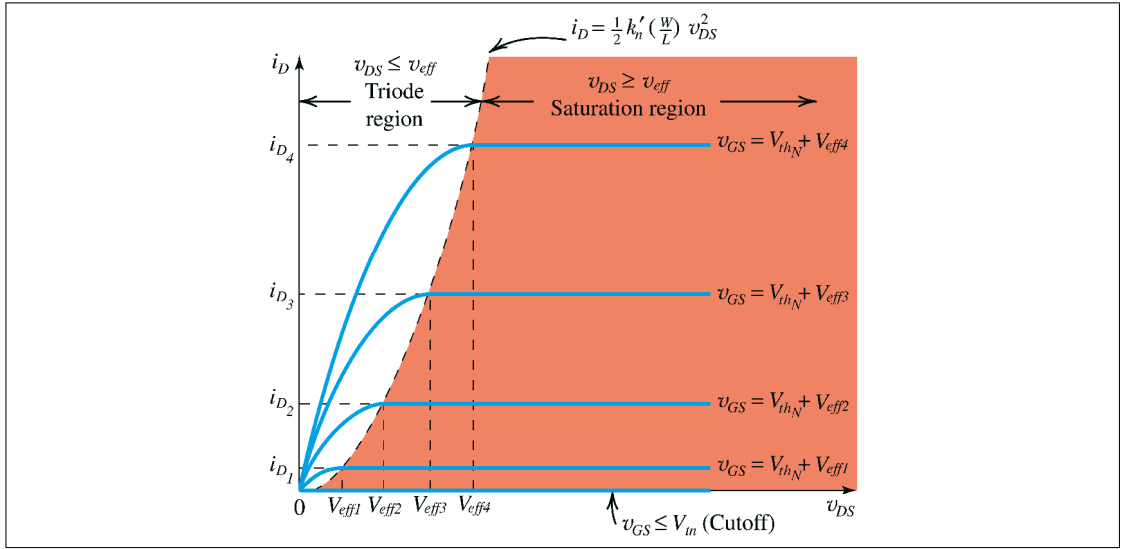


Figure 2.8: Enhancement-Type NMOS's $i_D - v_{DS}$ characteristic.

It is obvious that for various v_{GS} values, various V_{eff} will be acquired and Triode Region-Saturation Region boundary point will be shifted. However, since Triode Region-Saturation Region boundary point is defined by $v_{DS} = V_{eff}$, all boundary points resulted from variation of v_{GS} will be on the same curve which defined with this function:

$$i_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (v_{DS})^2 \quad (2.8)$$

These details about $i_D - v_{DS}$ characteristics of NMOS, which have explained above, are presented in Figure 2.8.

It should be noted that, in real applications or simulations based on real device models, NMOS's $i_D - v_{DS}$ resembles to the curve given in Figure 2.7 more than the given curve in Figure 2.8. However at that point this will be ignored.

2.5.2. Operation of PMOS

In Figure 2.2, physical structure of the P-Channel Enhancement-Type MOSFET's (PMOS) is presented. PMOS's operation bears a resemblance to the operation of NMOS. The only difference between them is in their physical structures. In opposition to NMOS's structure, in a PMOS, Drain and Source regions are consist of p-Type material and they are placed on top of a n-Type substrate. Consequently polarity of voltages applied on terminals of PMOS are exact opposite of the NMOS's. Thus, operation of NMOS and PMOS are complementary and these devices are called *Complementary Transistors*. Also, because of this difference in the physical structure, the channel of the PMOS consists of p-Type material and this is the reason why it is called *P-Channel MOSFET*.

To create a channel in PMOS for current flow, Gate terminal must be held at a lower level by V_{th_P} than Source terminal. In other words, following equation must be satisfied:

$$\begin{aligned} v_{GS} &\leq V_{th_P} \\ \text{or} \\ |v_{GS}| &\geq |V_{th_P}| \end{aligned} \tag{2.9}$$

In equation 2.9, v_{GS} and V_{th_P} has given as absolute values because it is considered useful to avoid confusion caused by signs of voltages applied to terminals of PMOS. In PMOS, direction of the current flow is from Source to Drain and it is carried by holes.

In order to create this current a negative V_{DS} must be applied. $i_D - v_{DS}$ characteristics of PMOS is presented in Figure 2.9.

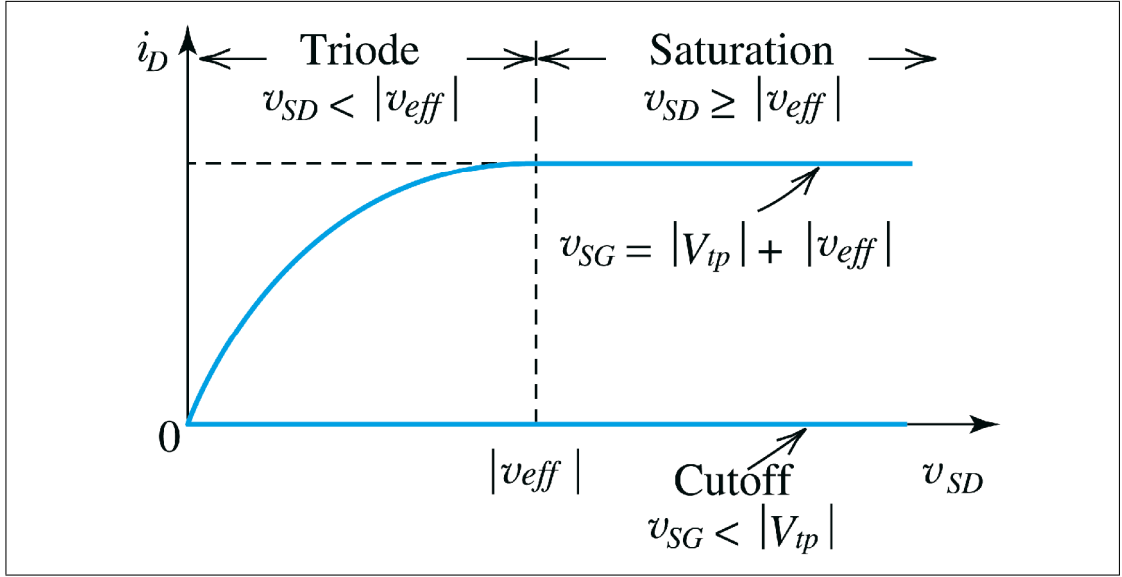


Figure 2.9: Enhancement-Type PMOS's $i_D - v_{DS}$ characteristic.

As mentioned previously, connecting NMOS's Bulk terminal to the lowest potential in the circuit to prevent internal pn junctions conduct current is a common practice in IC design. Same thing applies for PMOS either but in PMOS, in order to guarantee reverse bias on pn junctions, Bulk terminal should be connected to the highest potential in the circuit.

2.5.3. Predictive Technology Model (PTM)'s Characteristics

Within the scope of this study, 45nm High-Performance (HP) PTM MOSFET spice models will be used in the simulations. In this section, simulations and calculations take place in order to compare outcomes of the simulation results of PTM NMOS model's with the equations presented previously and show the consistency of simulation results. Reader may refer to Appendix A for details.

In Figure 2.10, a simple test circuit for 45nm HP PTM NMOS model is presented. Spice Netlist of this circuit has given in Appendix B. Here, V_{DD} voltage applied to the Gate and Bulk terminal is connected to $V_{SS} = 0V$. Also, output resistance r has chosen very small ($1m\Omega$).

In Figure 2.11a $i_D - v_{DS}$ curve of 45nm HP PTM NMOS model is presented. As can be seen in the figure, Saturation Region behaviour of this curve resembles with Figure 2.7 as mentioned earlier since it is a real device model. However, since within the scope of this study Triode Region operation is the only point of operation, this difference originated from the Channel Length Modulation will not be further examined.

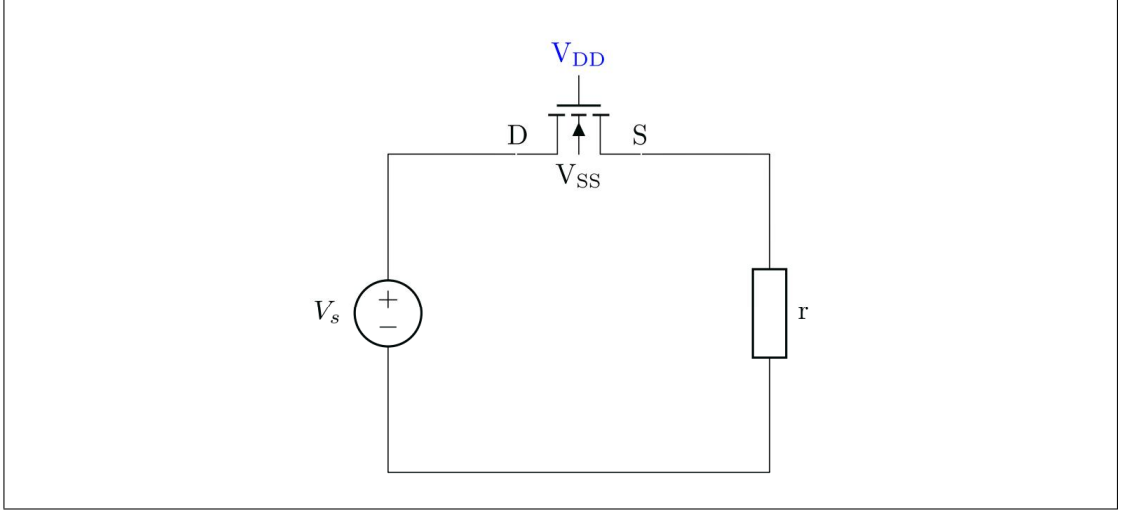


Figure 2.10: $i_D - v_{DS}$ test circuit of 45nm HP PTM NMOS model.

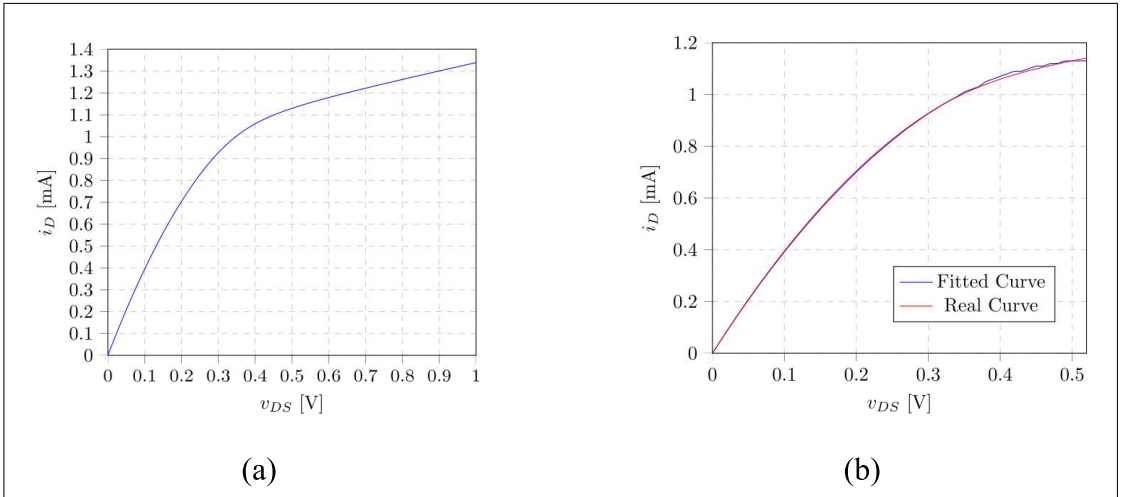


Figure 2.11: $i_D - v_{DS}$ curve of 45nm HP PTM NMOS model.

In Figure 2.11b, Triode Region portion of the $i_D - v_{DS}$ curve of PTM NMOS model's and a fitted curve is presented. Triode Region portion of the $i_D - v_{DS}$ curve has given with the equation 2.6. This equation can be organized as a second order polynomial:

$$\begin{aligned}
i_D &= \mu_n C_{ox} \left(\frac{W}{L} \right) \left(V_{eff} - \frac{v_{DS}}{2} \right) v_{DS} \\
&= \mu_n C_{ox} \left(\frac{W}{L} \right) \left(V_{eff} v_{DS} - \frac{(v_{DS})^2}{2} \right) \\
&= - \left[\mu_n C_{ox} \left(\frac{W}{L} \right) \frac{(v_{DS})^2}{2} \right] + \left[\mu_n C_{ox} \left(\frac{W}{L} \right) V_{eff} v_{DS} \right]
\end{aligned} \tag{2.10}$$

Equation of the fitted curve in Figure 2.11b is:

$$i_D = -0,00415 * v_{DS}^2 + 0,00433 * v_{DS} \tag{2.11}$$

Equalizing these two equation following results can be obtained:

- $\mu_n C_{ox} \left(\frac{W}{2L} \right) = 0,00415$
- $\mu_n C_{ox} \left(\frac{W}{L} \right) V_{eff} = 0,00433$

Since the values of $W = 1\mu m$ and $L = 0.045\mu m$:

- $\mu_n C_{ox} = 373,5\mu$
- $V_{eff} \approx 0,52168V$

It should be noted that, as given in model card of the PTM NMOS model, threshold voltage of the PTM NMOS when $V_{SB} = 0$ is $v_{th0} = 0,46893$ and as explained earlier $V_{eff} = v_{GS} - V_{thN}$. Thus calculated value of $V_{eff_{calc}}$ is:

- $V_{eff_{calc}} = v_{GS} - v_{th0} = 1V - 0,46893V = 0,53107V$

The difference between the calculated $V_{eff_{calc}}$ and the one extracted from the simulation output V_{eff} is:

- $V_{eff_{calc}} - V_{eff} = 0,53107V - 0,52168V \approx 0,009V$

Since there is a difference between the fitted curve and original curve and Body Effect is ignored, this difference can be considered natural. However, since this difference is smaller than 2% of the V_{eff} , it can be ignored.

There is another important parameter which can affect the operation of the MOS-FET either. This parameter is the (W/L) ratio, as known as *Aspect Ratio*. In Figure 2.12 change in the $i_D - v_{DS}$ curve is presented. As can be seen in the figure, with keeping the W constant, smaller L value causes steeper rise in $i_D - v_{DS}$ curve. In other words, as expressed in equation 2.6, W/L ratio is in direct proportion with i_D and simulation result is corroborating this equation.

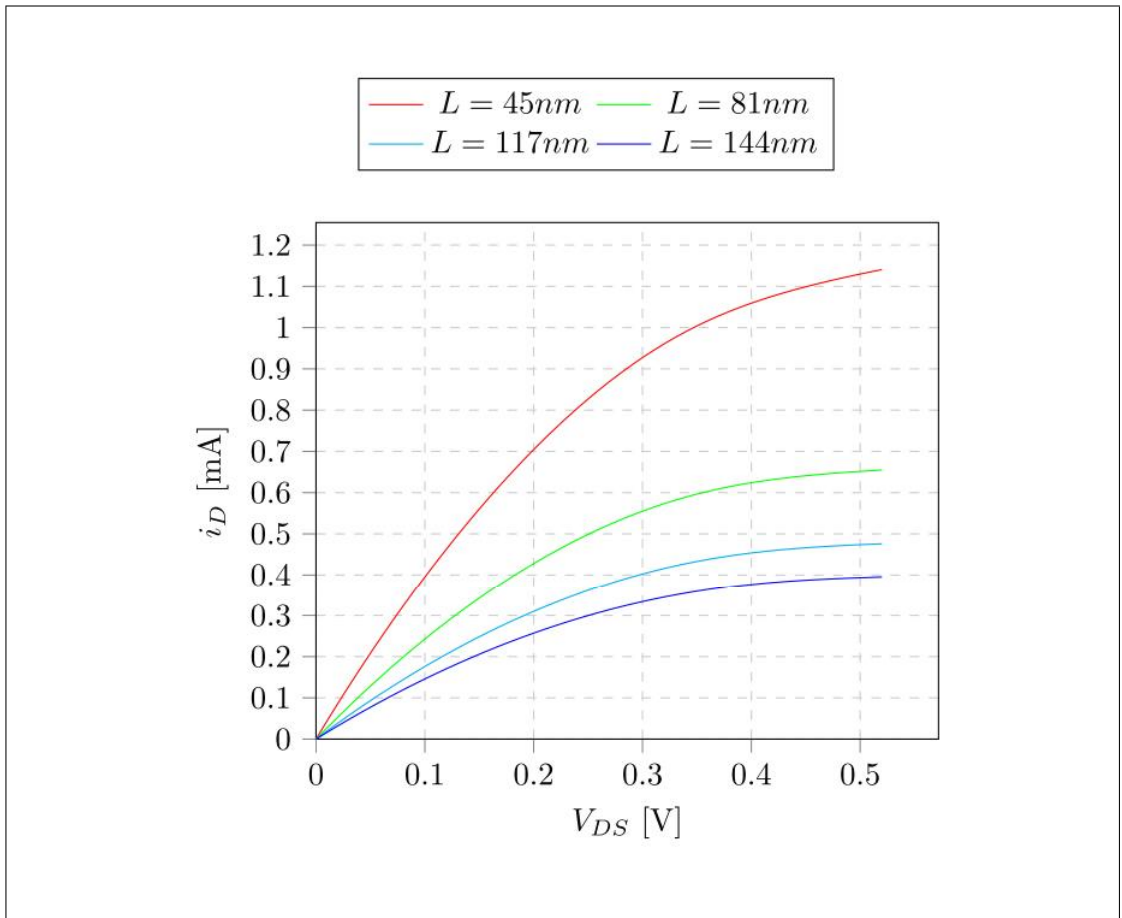


Figure 2.12: Change in the $i_D - v_{DS}$ curve against changing Aspect Ratio.

It should be noted that 45nm represents the minimum channel length (L_{min}) of NMOS and L values, which used in the simulation, must be equal or bigger than L_{min} .

Same analysis which mentioned above, applies for 45nm HP PTM PMOS spice model either. Besides the complementary voltage polarities and differences originated from these, operation principal of the PMOS is same with the NMOS.

In Figure 2.13, $i_D - v_{SD}$ curve of 45nm HP PTM PMOS model is presented. In this figure, max i_D value is about 2.9mA and in figure 2.11a it is about 1,35mA. Since $W_{NMOS} = 1\mu m$ and $W_{PMOS} = 3\mu m$, this difference is understandable.

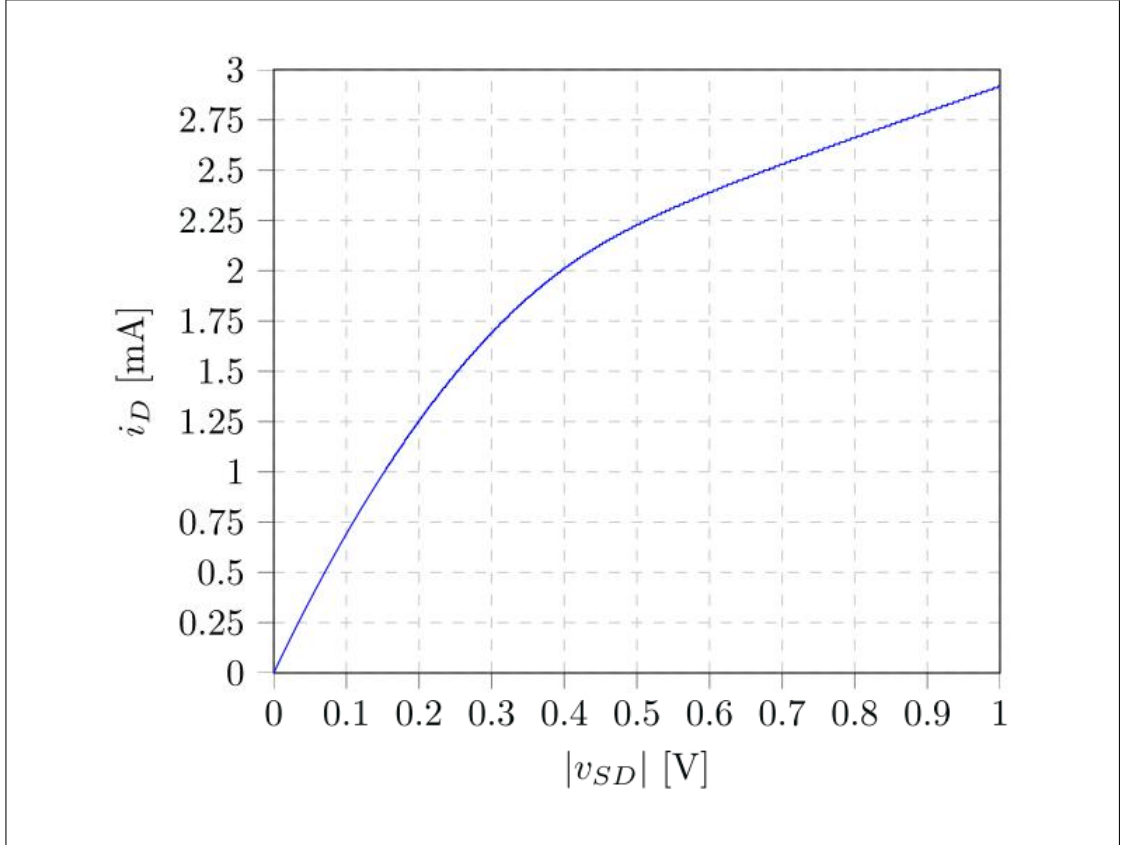


Figure 2.13: $i_D - v_{SD}$ curve of 45nm HP PTM PMOS model.

3. MOSFET SWITCHES

3.1. Introduction

In Figure 3.1, using ideal switch symbols, implementation of logical AND and OR functions are shown as examples. In Figure 3.1a, using two switches in series, logical AND function is carried out. In Figure 3.1b, logical OR function is carried out using two parallel switches.

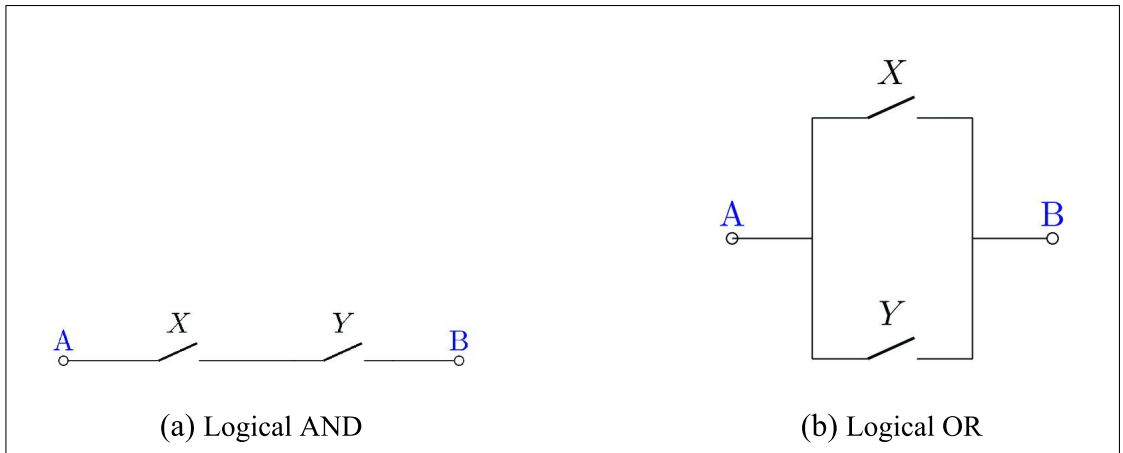


Figure 3.1: Implementation of logical functions with series and parallel switches.

An ON/OFF switch's single duty is to block or pass a signal. In this context, a MOSFET which is used as an ON/OFF switch is mentioned as *Pass Transistor* in literature and Pass Transistors are fundamental components of logic gates. It is possible to fulfill all logical functions with structures made out of parallel and series configurations of MOSFETs. However logic gates are not the only field which MOSFETs used as switches. Almost all modern ICs have MOSFET switches to fulfill certain functions. In the scope of this study, MOSFETs will be used in different applications rather than logic gates. Because of the various reasons, which are explained in Chapter 1, MOSFET has been chosen in order to implement switch function in these applications.

In this section, MOSFET switches will be explained in detail. It is considered necessary before starting analyze Switched-Capacitor circuits. Also, Pass Characteristics of NMOS and PMOS switches will be analyzed and their advantages and disadvantages will be explained either. Afterwards, performance of a structure called *CMOS Trans-*

mission Gate will be explained which consists of one NMOS and one PMOS. Finally performances, advantages and disadvantages of these three switches will be compared.

As explained in the previous chapter, in order to operate as an ON/OFF switch, MOSFETs must operate in Triode Region and Cut-Off Region. Therefore, further analyses regarding MOSFETs, will be solely made with regard to these two regions and Saturation Region operation of MOSFETs won't be mentioned unless it is absolutely necessary.

3.2. NMOS Switch

In order to analyze NMOS's pass characteristics, NMOS should be operating as a switch, in other words, should be operating either in Triode Region (ON State) or Cut-Off Region (OFF State).

While $V_{GS} < V_{th_N}$, NMOS operates in Cut-Off Region. In this region, NMOS does not conduct any current. In order to operate in Triode Region, $V_{GS} > V_{th_N}$ and $V_{DS} < V_{eff}$ equations must be satisfied. In this case i_D current flows through the NMOS.

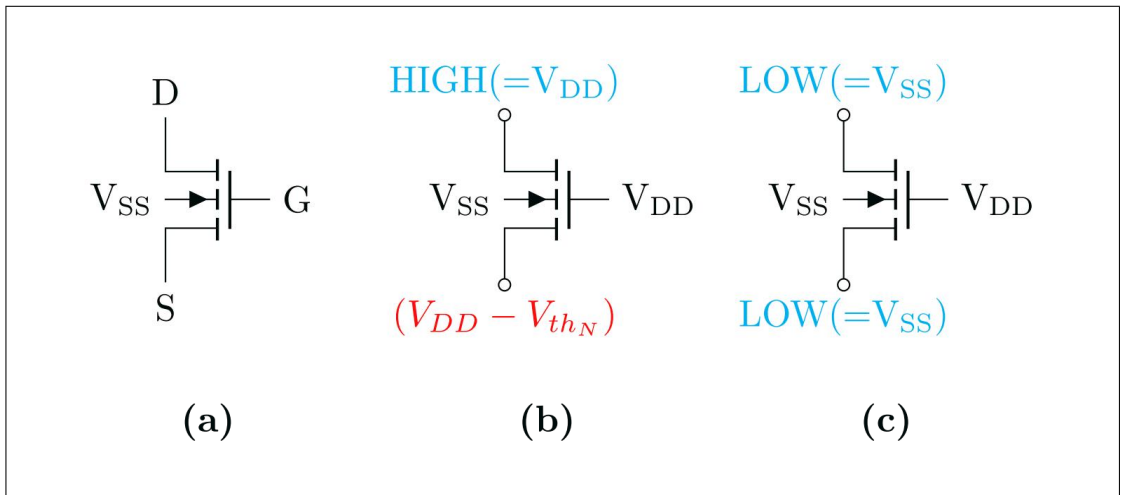


Figure 3.2: a) NMOS switch with b) HIGH level and c) LOW level passing characteristics of NMOS switch.

As mentioned earlier, when an NMOS used as an ON/OFF switch, it is expected to pass the signals, which applied to it's Drain terminal, to the Source terminal. The difference between the signal applied to the Drain and measured from the Source defines

it's performance and ideally it must be zero. As presented in Figure 3.2, while NMOS is ON, when a LOW (0V) level signal applied to its Drain, signal is passed to the Source without a loss and $V_{GS} > V_{th_N}$ is maintained. However, when a HIGH (V_{DD}) level is applied to the Drain of the NMOS, since V_S must be lower than the V_G at least by V_{th_N} and $V_G = V_{DD}$, V_S becomes:

$$V_S = V_{DD} - V_{th_N} \quad (3.1)$$

Thus, as is seen, NMOS displays a good performance passing LOW level but a poor performance passing HIGH level as a switch.

When MOSFET is operating in Cut-Off Region, presents a very high (typically bigger than $10^{12}\Omega$) channel resistance ($r_{DS_{OFF}}$) but when it is operating in Triode Region, presents a very low resistance (typically smaller than $10^3\Omega$) channel resistance ($r_{DS_{ON}}$).

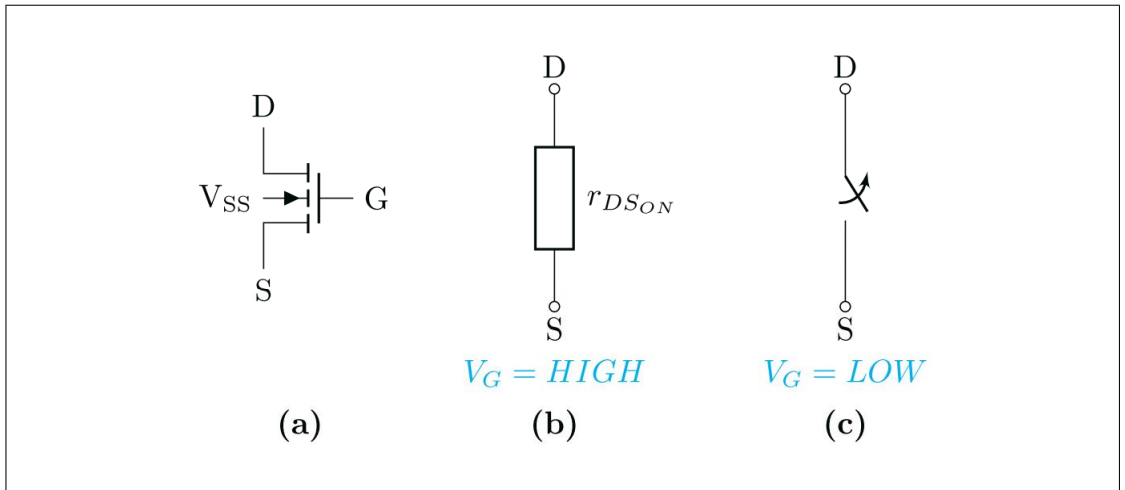


Figure 3.3: a) NMOS as a three terminal device, b) Equivalent drawing for NMOS in Triode Region and c) Equivalent drawing for NMOS in Cut-Off Region.

In Figure 3.3, equivalent drawings of an NMOS for both ON and OFF states presented. As simply presented in the Figure 3.3, when NMOS is OFF an $r_{DS_{OFF}}$ resistance occurs between Drain and Source terminals as mentioned earlier. Since $r_{DS_{OFF}}$ is extremely big comparing to $r_{DS_{ON}}$ and blocks current flow through the channel, in the figure, this resistance symbolized as open switch. When NMOS is ON, a small $r_{DS_{ON}}$ resistance observed is between Drain and Source terminals and it is presented as a res-

istance in the figure. Channel resistance of a MOSFET is one of the most important parameters which determines the performance and varies in direct proportion to Drain-Source voltage (V_{DS}).

As expressed in Chapter 1, NMOS's $r_{DS_{ON}} - v_{DS}$ curve changes in accordance with v_{DS} and V_{eff} . NMOS's $r_{DS_{ON}}$ characteristics has a great significance in its performance as a switch and it is desired to keep $r_{DS_{ON}}$ small as much as possible.

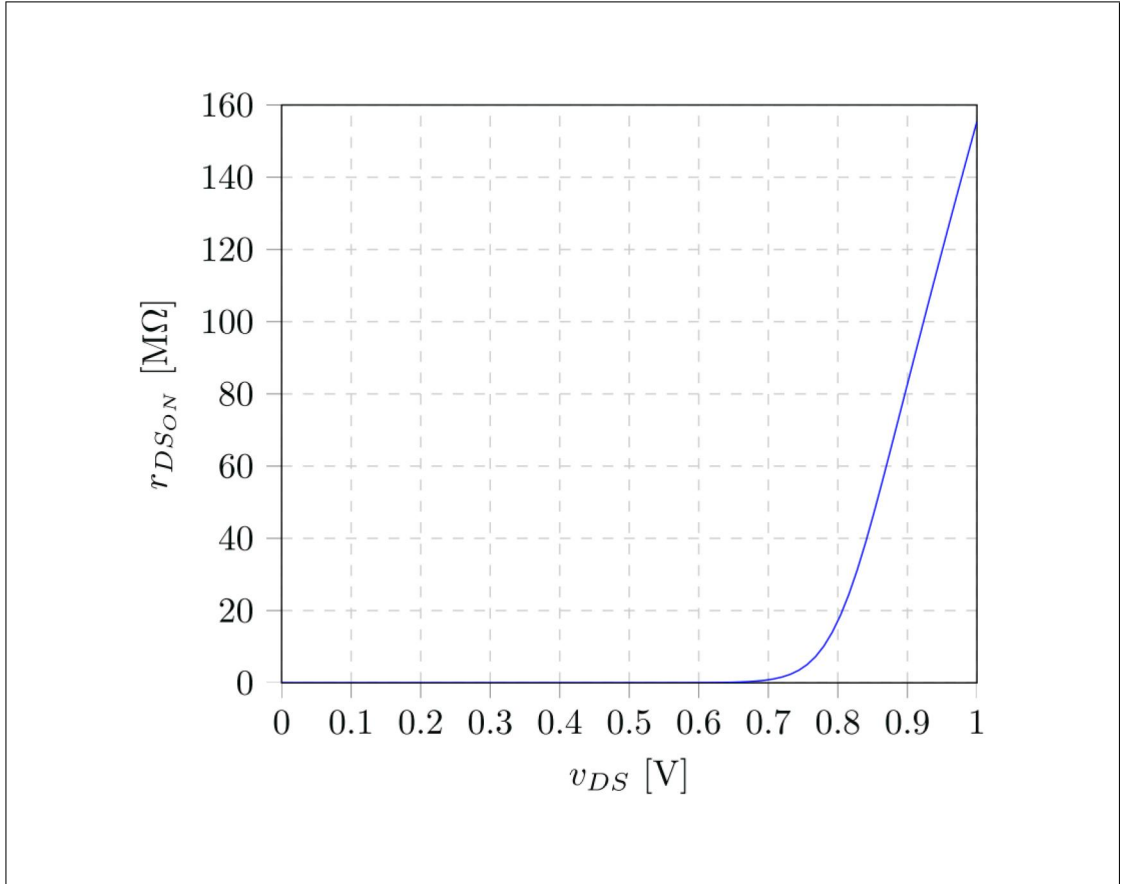


Figure 3.4: $r_{DS_{ON}} - v_{DS}$ curve of PTM NMOS model.

In Figure 3.4, $r_{DS_{ON}} - v_{DS}$ curve of PTM NMOS model is presented. Since

- $r_{DS_{ON}} = \frac{v_{DS}}{i_D}$

$r_{DS_{ON}}$ curve remains constant until NMOS goes into Saturation Region and after that point starts to rise as expected. In other words, as presented in Figure 2.11a, it is clear that while v_{DS} is increasing linearly, i_D follows it until $v_{DS} = V_{eff}$ point. Until that point $r_{DS_{ON}}$ remains constant after that point i_D remains constant and v_{DS} keeps rising, so $r_{DS_{ON}}$ start to increase with a steep slope.

3.3. PMOS Switch

The main difference between PMOS and NMOS is the polarities of the voltages which applied to the terminals of PMOS. For a PMOS, in order to operate in Cut-Off Region, the difference between Source voltage and Gate voltage should be smaller than threshold voltage, in other words $v_{SG} < |V_{th_P}|$ should be satisfied. In order to operate in Triode Region, $v_{DG} > |V_{th_P}|$ or $v_{SD} < |V_{eff}|$ should be satisfied.

As is the case with NMOS, in order to analyze PMOS's performance as an ON/OFF switch, difference between the signal which applied to it's Source (or input terminal) and the signal which measured from it's Drain (or output terminal) should be observed. In ideal, signal should be passed right through PMOS without any loss. Same as NMOS, PMOS blocks signal completely when it is OFF. Thus, in order to characterize it's performance as an ON/OFF switch, it's passing character should be analyzed when it is ON, in other words, while operating in Triode Region.

When PMOS is ON, current flows from Source to Drain because of the voltage polarities. In order to make a PMOS switch ON, it's Gate voltage must be held lower than it's Drain at least by $|V_{th_P}|$. PMOS's pass characteristics is presented in the case Gate voltage is LOW and PMOS is ON in the equation below.

PMOS Pass Characteristics:

$$I.V_S = HIGH \implies V_D = V_{DD} \quad (3.2a)$$

$$II.V_S = LOW \implies V_D = v_G + |V_{th_P}| = |V_{th_P}| \quad (3.2b)$$

As presented in expressed in Equation 3.2a, when voltage applied to the Source terminal of PMOS is HIGH, voltage measured from the Drain terminal is HIGH either. In this case both $v_{GD} < |V_{th_P}|$ and $v_{SG} > |V_{th_P}|$ equations are satisfied. However, when the Source voltage is switched to LOW, the Gate voltage has to be lower than the Drain voltage by $|V_{th_P}|$, Drain voltage value cannot be smaller than $|V_{th_P}|$. In this case, it is obvious that PMOS is not showing a good performance passing LOW level. Thus, as an ON/OFF switch, PMOS shows a good performance passing HIGH level but poor performance passing LOW level. Passing characteristics of PMOS visualized in Figure 3.5.

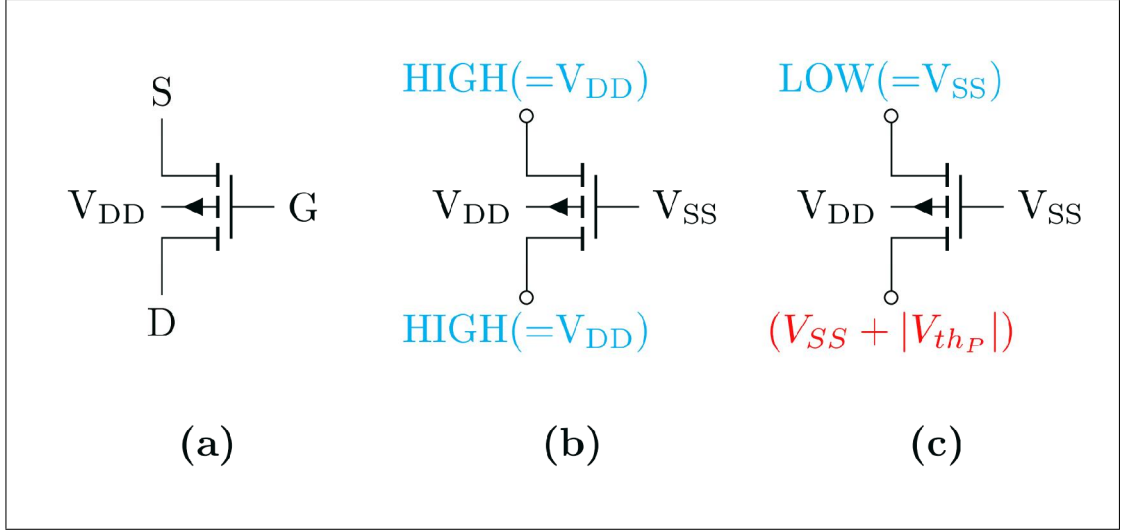


Figure 3.5: a) PMOS switch with b) HIGH level and c) LOW level passing characteristics of PMOS switch.

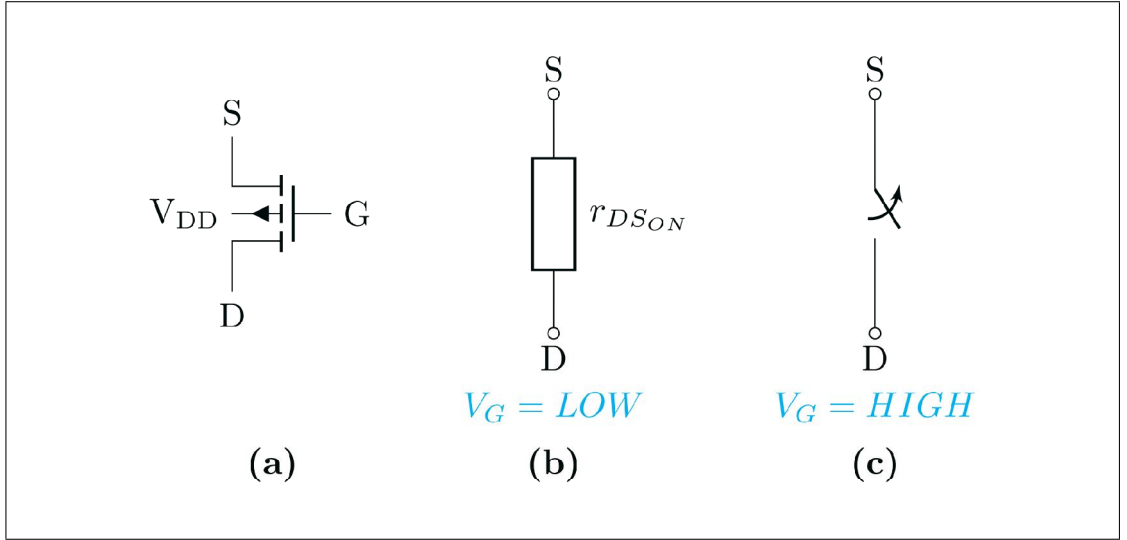


Figure 3.6: (a) PMOS as a three terminal device, (b) Equivalent drawing for PMOS in Triode Region and (c) Equivalent drawing for PMOS in Cut-Off Region.

In addition, same as NMOS, PMOS exhibits a very big resistance when it is OFF ($r_{SD_{OFF}}$) and a very small resistance when it is ON ($r_{SD_{ON}}$) between Source and Drain. As mentioned in the previous section, this resistance values are very important parameters in context of passing characteristics of PMOS. This resistances are visualized as simple equivalents in Figure 3.6 and $r_{DS_{ON}} - v_{DS}$ curve of PTM PMOS model is presented in Figure 3.7.

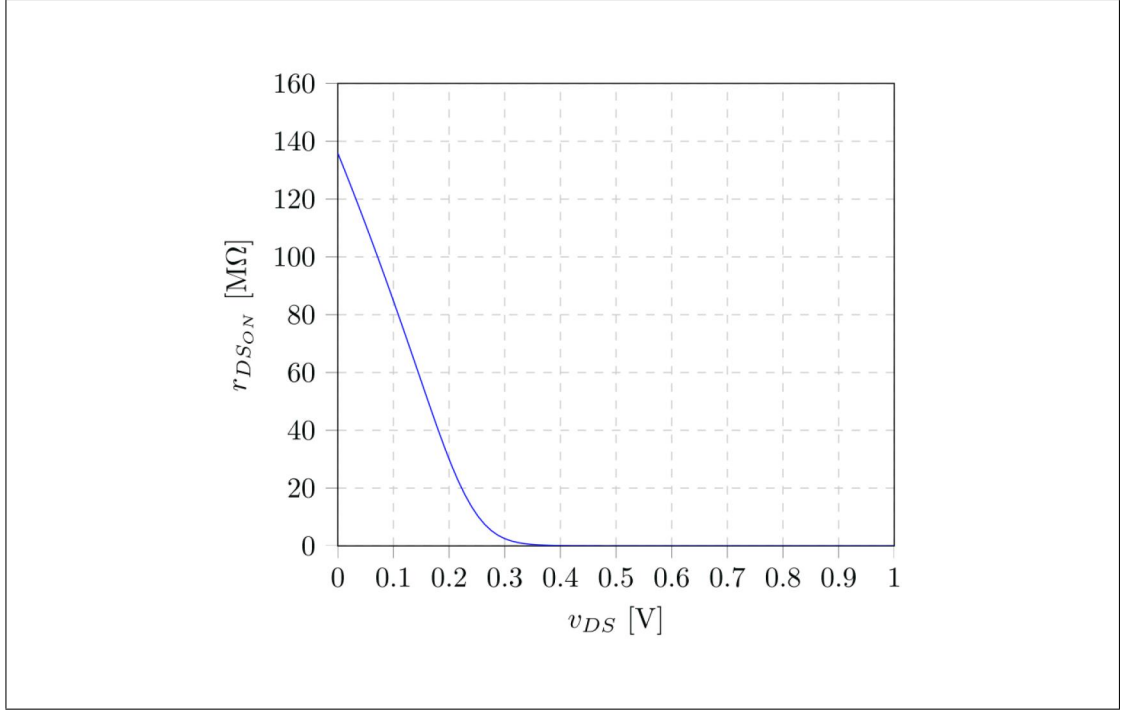


Figure 3.7: $r_{DS(on)} - v_{DS}$ curve of PTM PMOS model.

3.4. Transmission Gate

Transmission Gate (or CMOS Transmission Gate), is a structure which does not suffer disadvantages that NMOS and PMOS have. Also it shows a much more better performance as a switch at passing both HIGH and LOW levels. Transmission Gate comprises of one NMOS and one PMOS which are connected as presented in Figure 3.8.

As explained earlier, when NMOS is ON and a HIGH(V_{DD}) level applied to it's Drain, it's Source voltage becomes $V_{DD} - V_{th_N}$. In other words, if a capacitor connected to the Source of the NMOS, it can be charged only up to $V_{DD} - V_{th_N}$. However, since PMOS is good at passing HIGH level, Transmission Gate compensates that difference between Drain and Source with PMOS and charges this capacitor to the HIGH level. When NMOS stops charging capacitor when it's voltage reached $V_{DD} - V_{th_N}$ PMOS takes over and charges the capacitor. Same operation applies for LOW level input signal either. In Figure 3.9 pass characteristics of 45nm HP PTM NMOS and PMOS models.

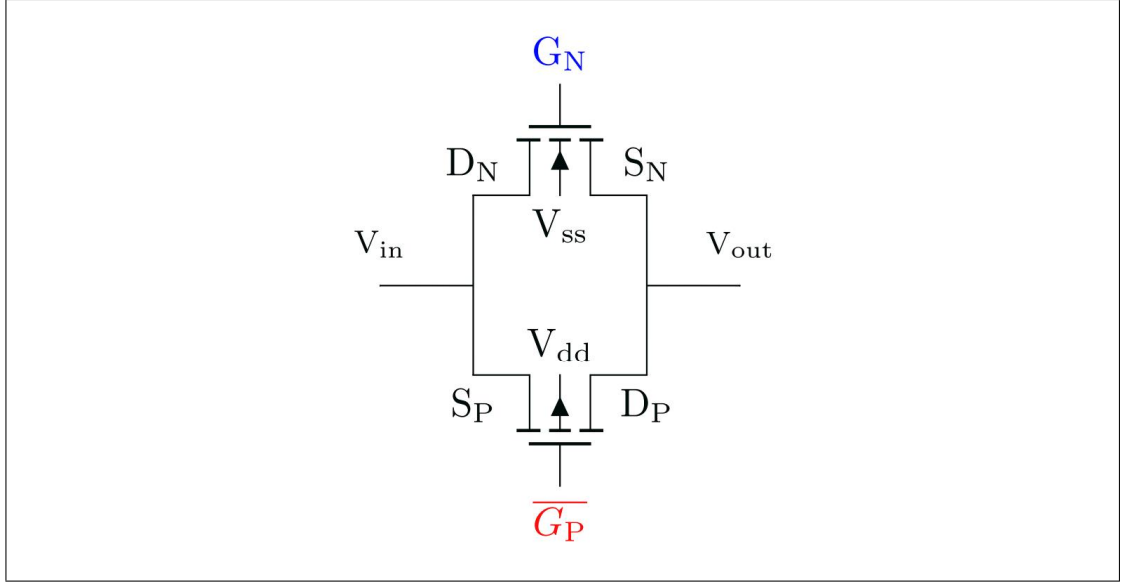


Figure 3.8: CMOS Transmission Gate.

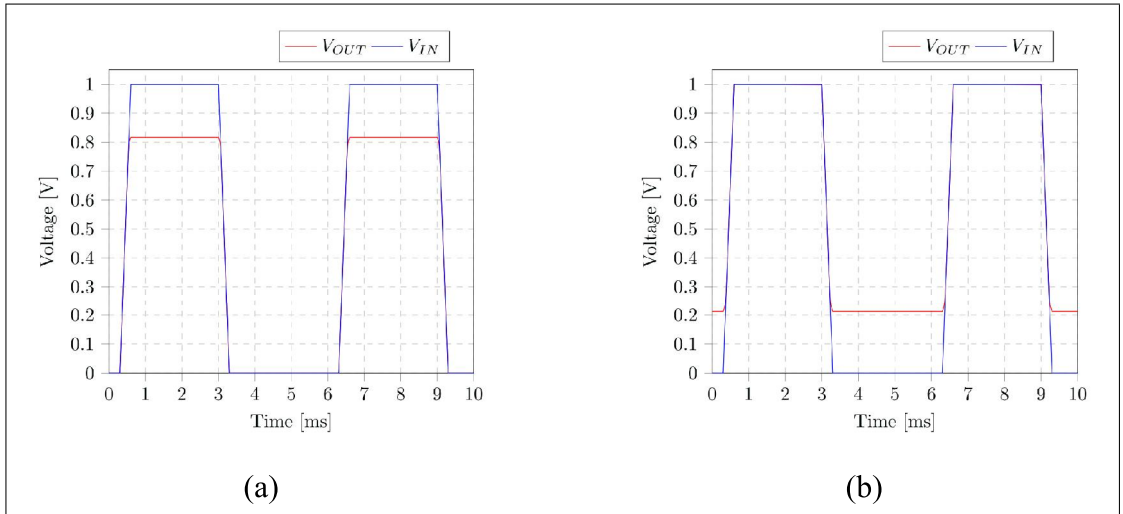


Figure 3.9: Pass characteristics of PTM a) NMOS and b) PMOS models.

In Figure 3.10 pass characteristics of Transmission Gate created with 45nm HP PTM NMOS and PMOS. It can be seen in the figure that it passes both HIGH and LOW levels without any attenuation as explained earlier.

As presented in Figure 3.11, there is a direct proportion between r_{SDON} and V_{DS} of the NMOS but inverse proportion between r_{SDON} and V_{DS} of the PMOS. Because of the structure of Transmission Gate, r_{SDON} of NMOS and PMOS becomes parallel while Transmission Gate is ON. Thus, Transmission Gate's r_{SDON} becomes almost constant throughout the whole V_{DS} range. Also, as can be seen in Figure 3.11, r_{SDON}

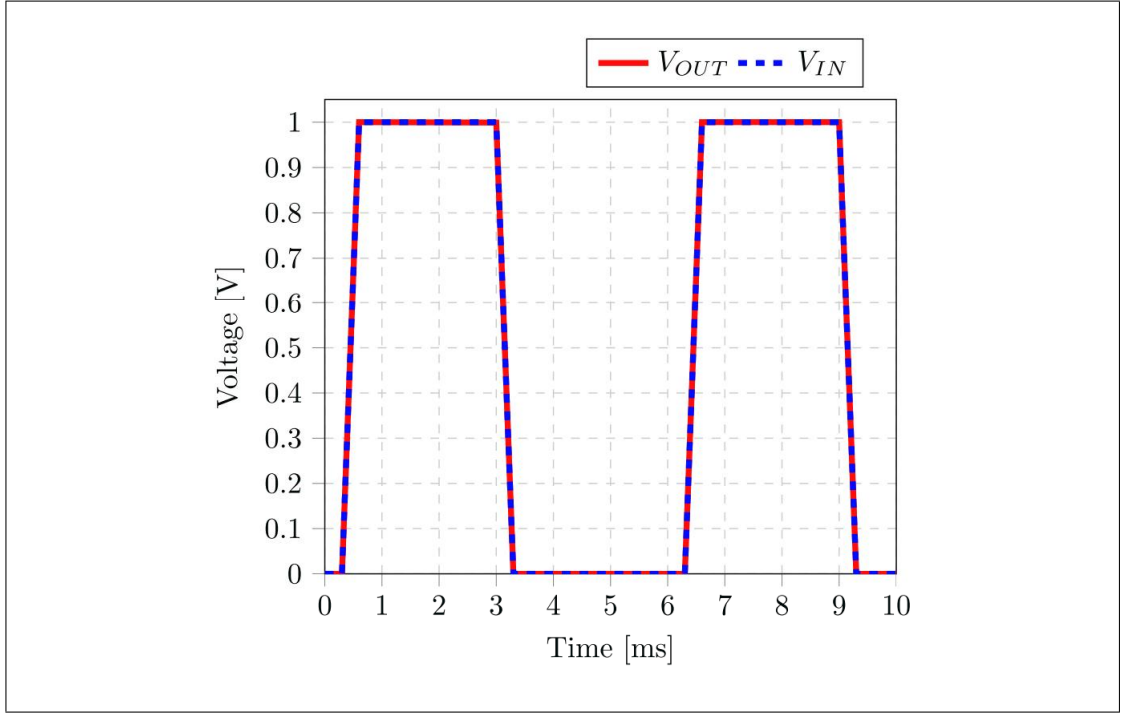


Figure 3.10: Pass characteristics of Transmission Gate created with 45nm HP PTM NMOS and PMOS.

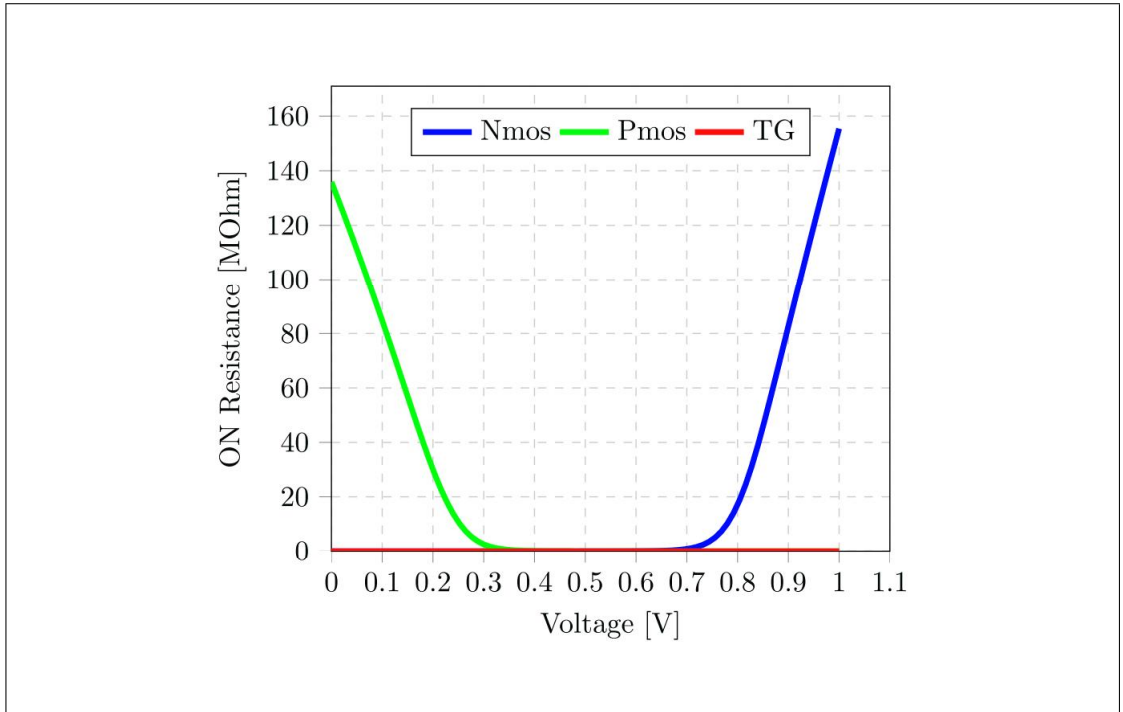


Figure 3.11: NMOS, PMOS and Transmission Gate $r_{DS_{ON}}$ comparison.

of Transmission Gate's is typically much smaller than NMOS's and PMOS's. These advantages of Transmission Gate can be formulated as:

$$r_{DS_{ONeq}} = \frac{r_{DS_{ONN}} r_{DS_{ONP}}}{r_{DS_{ONN}} + r_{DS_{ONP}}} \quad (3.3)$$

In Figure 3.11, $r_{SD_{ON}}$ of Transmission Gate presented as zero but this its actual value is in the range of $5k\Omega$ - $20k\Omega$. However, comparing to NMOS's and PMOS's $r_{SD_{ON}}$ values, which are in the range of $20k\Omega$ - $140M\Omega$, it can be considered as zero. These $r_{SD_{ON}}$ values can be adjusted by changing parameters such as W/L ratio or V_{DD} .

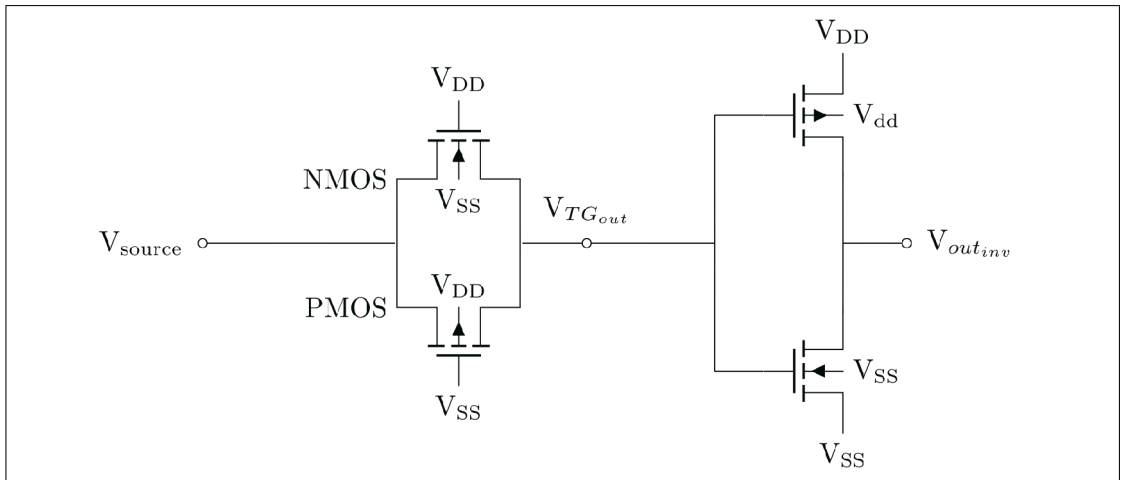


Figure 3.12: Test circuit for Transmission Gate's $r_{DS_{ON}}$.

In Figure 3.12, test circuit which is designed in order to obtain Transmission Gate's $r_{DS_{ON}}$ is presented. In this circuit and other test circuits, which are used in order to obtain NMOS's and PMOS's $r_{DS_{ON}}$ plots, CMOS Inverters used as load. CMOS Inverter provides a light and fast switching load. Besides, in order to provide a load for both NMOS and PMOS, this configuration is necessary.

4. SWITCHED-CAPACITOR

4.1. Introduction

Resistors are one of the fundamental components of electronic circuits. Resistors are used as discrete components while designing a circuit but in IC design these components have to be made out of semiconductor materials and have to be packed with the rest of the circuit in a single chip. Semiconductor resistors which are placed in an IC occupy very large area in comparison with MOSFET. As scientists' one of the biggest goal is to create larger circuits in smaller size since the invention of the semiconductor IC technology, this is considered as a major problem in context of IC design. In addition, in applications such as instrumentation or audio, it is highly desired to use components which have tolerance values under 1% and have very good thermal stability. However it is not possible to manufacture semiconductor resistors with this accuracy because of deviations in the process and fabrication parameters. These kind of problems have forced scientists to come up with new solutions and switched-capacitor structure is the most common solution for that. [4],[7],[12]

Principles of the *Switched-Capacitor* structure dates back to almost 150 years. In 1873, James Clerk Maxwell has been presented an analysis, which offers a method to measure a capacitor's value, in his publication (see [11]). This analysis describes a capacitor's behaviour when changing its polarity right after it is fully charged. Afterwards Maxwell confirms that if this switching is repeated periodically then this capacitor behaves like a resistor with value of T/C . Thus, he figures that it is possible to calculate capacitor's value by first measuring the average voltage and average current, then using the frequency of this switching capacitor's value can be obtained. However publishing of first theoretical studies and applications took almost a century after Maxwell's this analysis. As a matter of fact at early studies in this topic, researchers did not relate their work with Maxwell's despite the fact that he is the one who found the principal of the Switched-Capacitor. For example David L. Fried mentioned this structure in his paper, which has been published in 1972 at IEEE Journal of Solid States Circuits, as (see [5]) [20]:

"A rather interesting and previously unrecognized filter-design concept"

In this chapter, at first, Switched-Capacitor application which called as *Switched-Capacitor Resistor* will be explained and analyzed. Afterwards, various applications which use switched-capacitor resistor as a replacement will be examined.

4.2. Switched-Capacitor Resistor

In reality, switches that is used in switched-capacitor ICs are comprise of semiconductor switches or structures which use more than one semiconductor switch. Because of many advantages, which are explained in the first chapter, MOSFET's are the most common choice for such applications. Again, as explained in the first chapter, CMOS Transmission Gate is the best performing semiconductor switch among three and this will be used in following applications.

A Switched-Capacitor Resistor is a structure which simulates resistor behaviour and operates as an programmable equivalent resistor. This structure offers a resistor function with lower cost, higher accuracy, lesser external component and higher temperature stability. Because of these advantages, they are widely used in modern ICs which can offer various functions such as filtering, data converting, analog, digital and mixed-signal processing on single chip. However, the biggest disadvantages of switched-capacitor circuits is the high switching noise. [4],[7],[12]

In order to explain fundamentals of this structure, first ideal switches will be used. Afterwards, these will be replaced with the Transmission Gates and Transmission Gates will be used in following applications instead of ideal switches. The term of "Ideal Switch" can be described as; an SPST (Single-Pole Single-Throw) switch which has zero delay when an ON or OFF signal is applied and presents zero resistance while it is conducting.

In Figure 4.1a, fundamental switch-capacitor resistor structure, which comprises of two ideal switches and one capacitor, is presented. This is the structure which will be used in this study. There are various switched-capacitor resistor structures, which comprise of more than two switches with various configurations, but in order to estab-

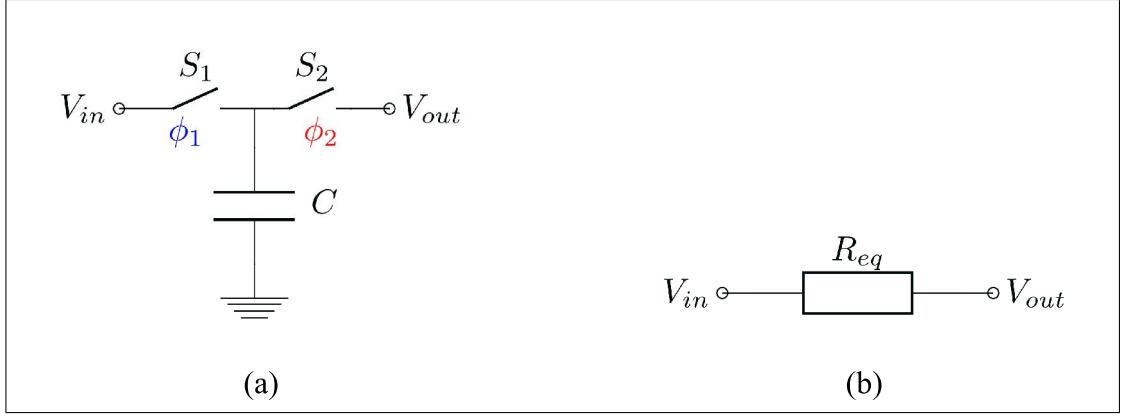


Figure 4.1: a) The Switched-Capacitor resistor using ideal switches and b) Equivalent resistor.

lish a fundamental grasp on the applications, which are the subject of this study, this simple structure has been chosen.

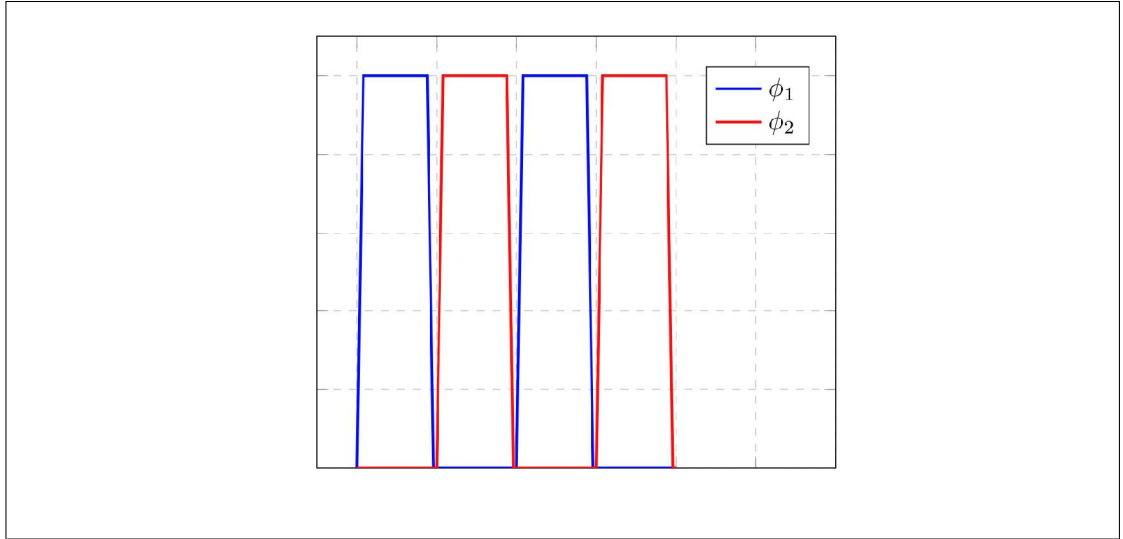


Figure 4.2: Non-overlapping switching signals.

S_1 and S_2 switches in the Figure 4.1a are driven with the non-overlapping drive signals presented in Figure 4.2. In other words, while S_1 is ON S_2 is OFF and vice versa. Since in reality there will be delays at the transition between ON and OFF states and in addition to that there will be some time needed in order discharge of the internal capacitors of the MOSFETs, a *Dead-Time* must be placed between switching signals.

4.2.1. Operation of the Switched-Capacitor Resistor

At the circuit presented in Figure 4.1a, S_1 switch charges up the capacitor when it is ON and $V_i > 0$ at the same time. Value of the charge accumulated on the capacitor at that moment is given by:

$$Q = V_i * C \quad (4.1)$$

[12],[13]

When S_1 switches to the OFF state and S_2 switches to the ON state, charge on the capacitor starts to flow to the output and C discharges. If these switching between ON and OFF states become repetitive then charging and discharging of the capacitor becomes repetitive either. If this switching repeats with the period of T_{CLK} then:

$$I_{avg} = \frac{q}{T_{CLK}} = \frac{V_i * C}{T_{CLK}} = V_i * C * f_{CLK} \quad (4.2)$$

[12],[13]

So equivalent input resistance can be expresses as:

$$R_{eq} = \frac{V_i}{I_{avg}} = \frac{V_i}{V_i * C * f_{CLK}} = \frac{1}{C * f_{CLK}} \quad (4.3)$$

[12],[13]

It is clear that R_{eq} value depends on C and f_{CLK} . If C is kept constant, value of R_{eq} can be adjusted by changing the f_{CLK} . This feature of switched-capacitor resistors, able to change R_{eq} value in a wide range by only changing the switching frequency, is another big advantage. [12]

In switched-capacitor circuits, switching frequency (f_{CLK}) must be very big comparing to the source frequency (f_{source}):

$$f_{CLK} \gg f_{source} \quad (4.4)$$

In other words, in order to reflect every change which occurs in the source signal to the output, switches must be too much faster than the source. Thus transfer of charge packets from source to output can be considered a continuous flow of current. Besides,

by increasing the switching frequency capacitor size can be decreased and still same R_{eq} value can be obtained. Thereby, with smaller capacitor, area occupied in IC can be reduced. However, increasing switching frequency too much can introduce noise related problems and since occupied die area in an IC and internal parasitic capacitances dictates the upper and lower limits of the capacitor values design trade-offs must be done.

4.3. Switched-Capacitor Low-Pass Filter

In electronics, a filter is defined as a structure which passes or blocks a signal according to its frequency. Such as High-Pass or Low-Pass they are denominated according to their passing characteristics. For example, a Low-Pass filter passes signals which have frequency under a certain frequency value and blocks signals which have bigger frequency than this certain frequency. However, characteristic behaviour of the high-pass filter is passing high frequency signals and rejecting low frequency signals. This certain frequency which is a threshold point that the filter changes its behaviour is called *Cut-Off Frequency* or *Corner Frequency*.

Also, filters which comprise of active components such as transistors or operational amplifiers are called *Active Filters* and which comprise of passive components such as resistor or capacitor are called *Passive Filters*. The definition of 'Active' and 'Passive' is based on whether a component is need a source to operate or not. In addition, order of a filter is another denominator which provides information about filter's characteristics. Filters which have single reactive component are called *First-Order* or *One-Pole* or *Single-Pole* filters. In this section a First-Order RC Low-Pass filter and its Switched-Capacitor equivalent will be presented.

According to definition of the ideal filter, filters behaviour immediately changes at the cut-off frequency without a delay in the transition or attenuation in the signal. Thus, for example in a Low-Pass filter, if input signal's frequency is smaller than the cut-off frequency then signals passes right through the filter without loss and delay. However if the input signal's frequency increases filter blocks it at the moment its frequency reaches the cut-off frequency. However in reality filters does not respond that fast

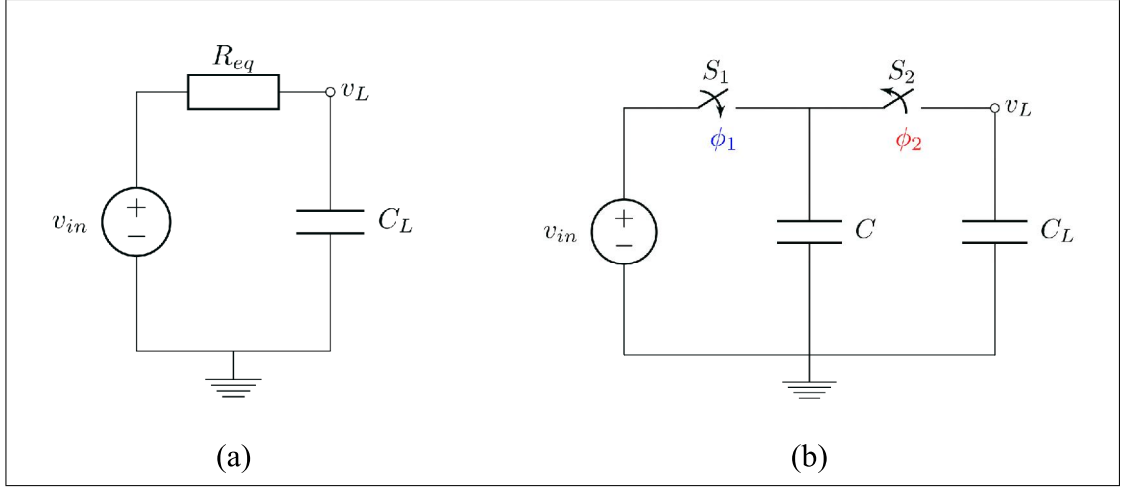


Figure 4.3: a) First Order RC and b) Switched-Capacitor Low-Pass filter circuits.

and they also cause some attenuation and phase shift in the signal. In other words, filters have different gains for different frequency components and they also may cause attenuation even before the cut-off frequency. In addition, it should be noted that filters do not add new components in the signals.

In figure 4.3a, a First-Order RC Low-Pass filter is presented. In the equation below, this filter's cut-Off frequency is presented:

$$f_c = \frac{1}{2\pi\tau} = \frac{1}{2\pi RC}$$

or

$$\omega_0 = \frac{1}{\tau} = \frac{1}{RC}$$
(4.5)

Its frequency response is given by this equation:

$$H(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{1 + j\omega RC} = \frac{1}{1 + \frac{j\omega}{\omega_0}}$$
(4.6)

First-Order RC Low-Pass filter's gain is:

$$Gain = 20\log \frac{V_{out}}{V_{in}}$$
(4.7)

At the cut-off frequency, input signal's gain decreases to $-3dB$ and after that point keeps decreasing with a slope of $-20dB/Decade$. Also, at the cut-off frequency, phase of the input signal shifts -45° .

In order to simulate the circuit presented in 4.3a and compare the simulation results with Low-Pass filter characteristics, first some values must be given for the capacitor and the resistor in the circuit and cut-off frequency must be calculated. Second, this circuit must be simulated using the same values and results must be compared. To this end, resistor and capacitor values have chosen $R = 10k\Omega$ and $C = 159.1549nF$. These certain values have chosen in order to obtain a convenient cut-off frequency. In this case, cut-off frequency is:

$$\bullet f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi * 10k\Omega * 159.1549nF} \approx 100Hz$$

In Figure 4.4 Bode Plot is presented as the result of the simulation. In this simulation frequency range between $1Hz$ and $1MHz$ are swept. As described earlier, it can be seen in the figure that gain has decreased approximately to $-3dB$ and kept decreasing with a slope of $-20dB/Decade$ at the cut-off frequency. Also phase shift at that frequency is -45° as explained.

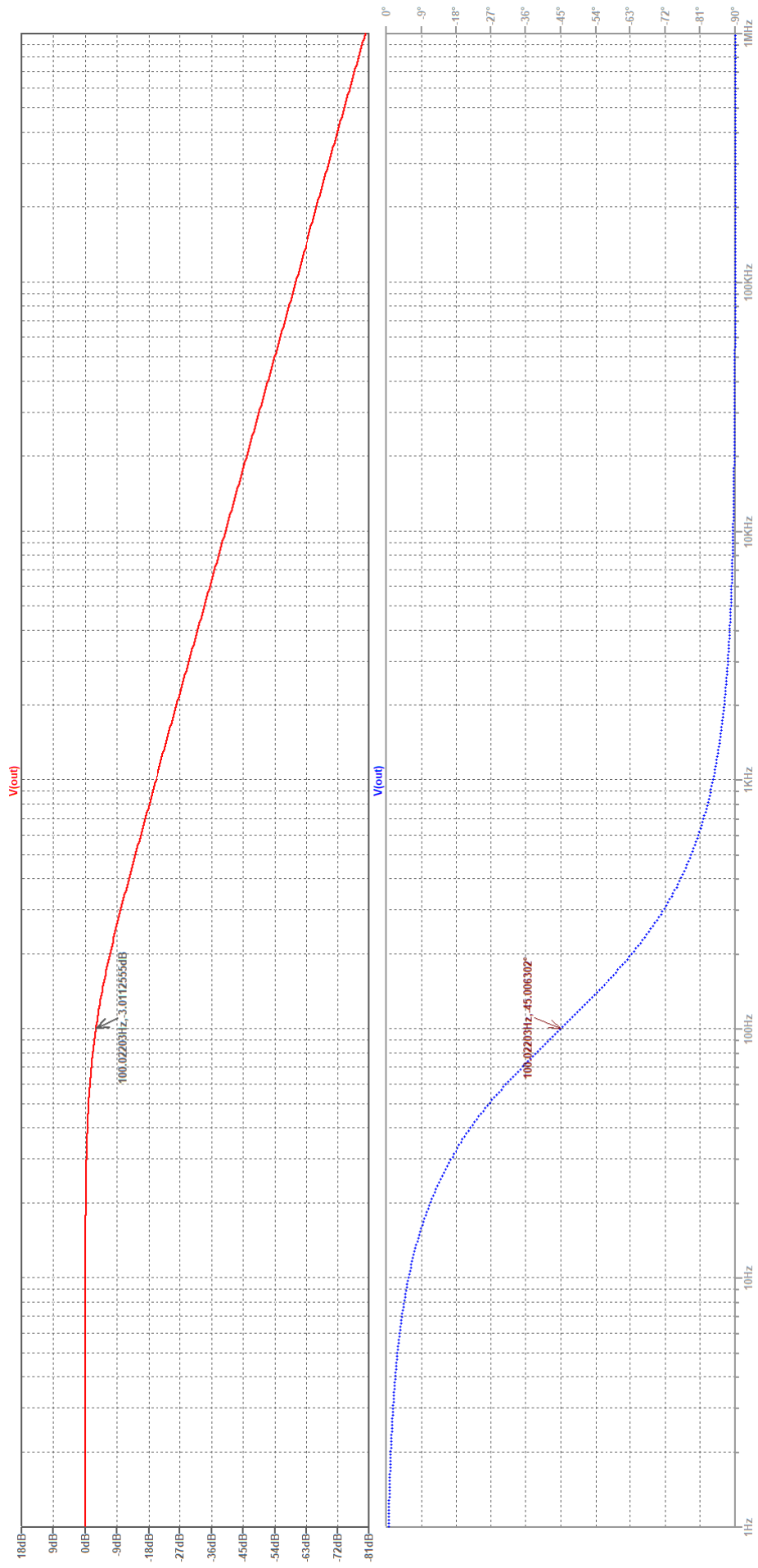


Figure 4.4: First-Order RC Low-Pass Filter's Frequency Response.

If the same circuit and same components values are used and an sinusoidal input signal with a 1V amplitude and 100Hz frequency applied, amplitude and phase of the input voltage changes at the output. In Figure 4.5, simulation results of this circuit is presented.

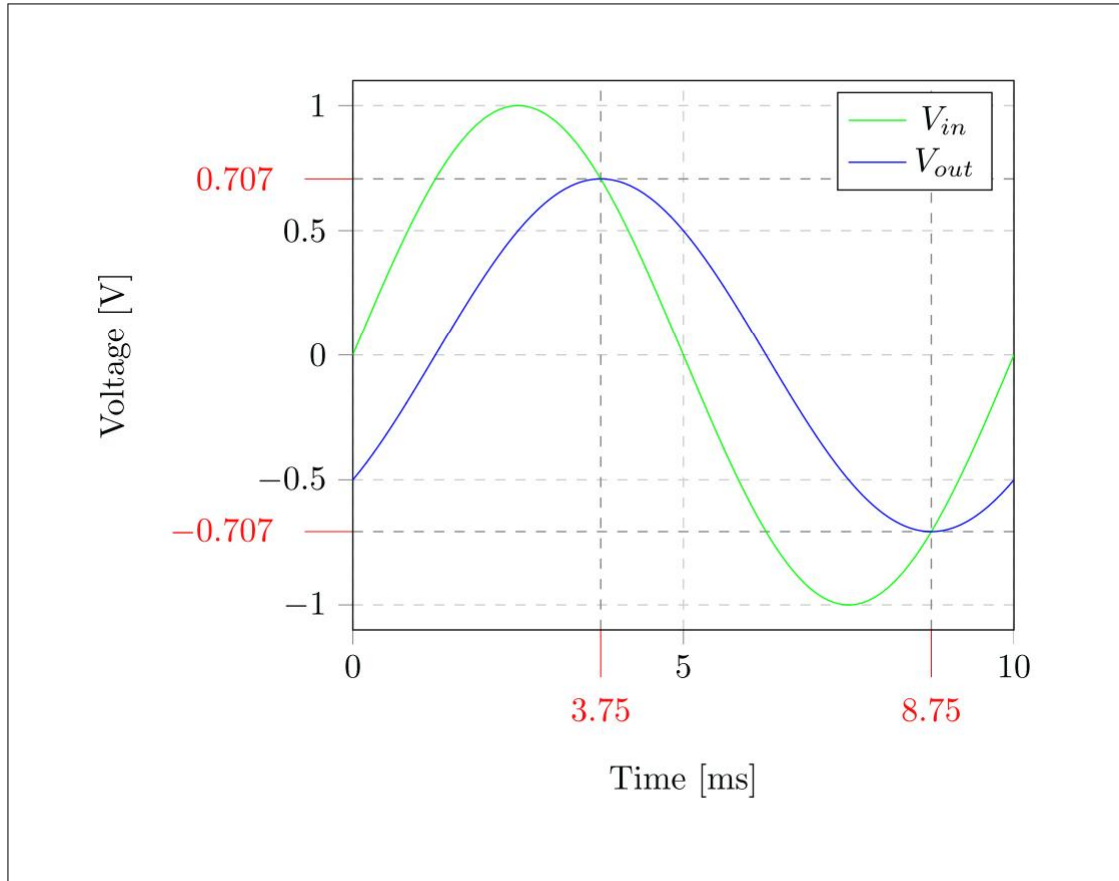


Figure 4.5: Input voltage vs output voltage of First-Order RC Low-Pass filter.

As presented, output voltage's peak value is 0.707V despite fact that input voltage is 1V. It can be confirmed by using the equation 4.7:

- $Gain = 20\log \frac{V_{out}}{V_{in}}$
- $Gain = 20\log \frac{0.707V}{1V}$
- $Gain \approx -3dB$

Also, since two signals in the Figure 4.5 is not overlapping, phase shift can be observed.

If the resistor in the RC Low-Pass circuit presented in the Figure 4.3a is replaced with a Switched-Capacitor Resistor, the circuit in the Figure 4.3b is obtained. As mentioned earlier, switched-capacitor resistor replicates resistor's behaviour, so it is expected to obtain same results when this circuit is simulated. Since $R_{eq} = 10k\Omega$, by determining f_{CLK} and C values, simulation setup can be completed. Thus, from 4.3 and 4.4;

- $f_{CLK} = 100 * f_{source}$
- $R_{eq} = \frac{1}{C * f_{CLK}} \rightarrow C = \frac{1}{R_{eq} * f_{CLK}} = \frac{1}{10k\Omega * 10kHz} = 10nF$

Simulation results obtained from the Switched-Capacitor Low-Pass circuit, which comprise of components that have calculated values above, is presented in Figure 4.6.

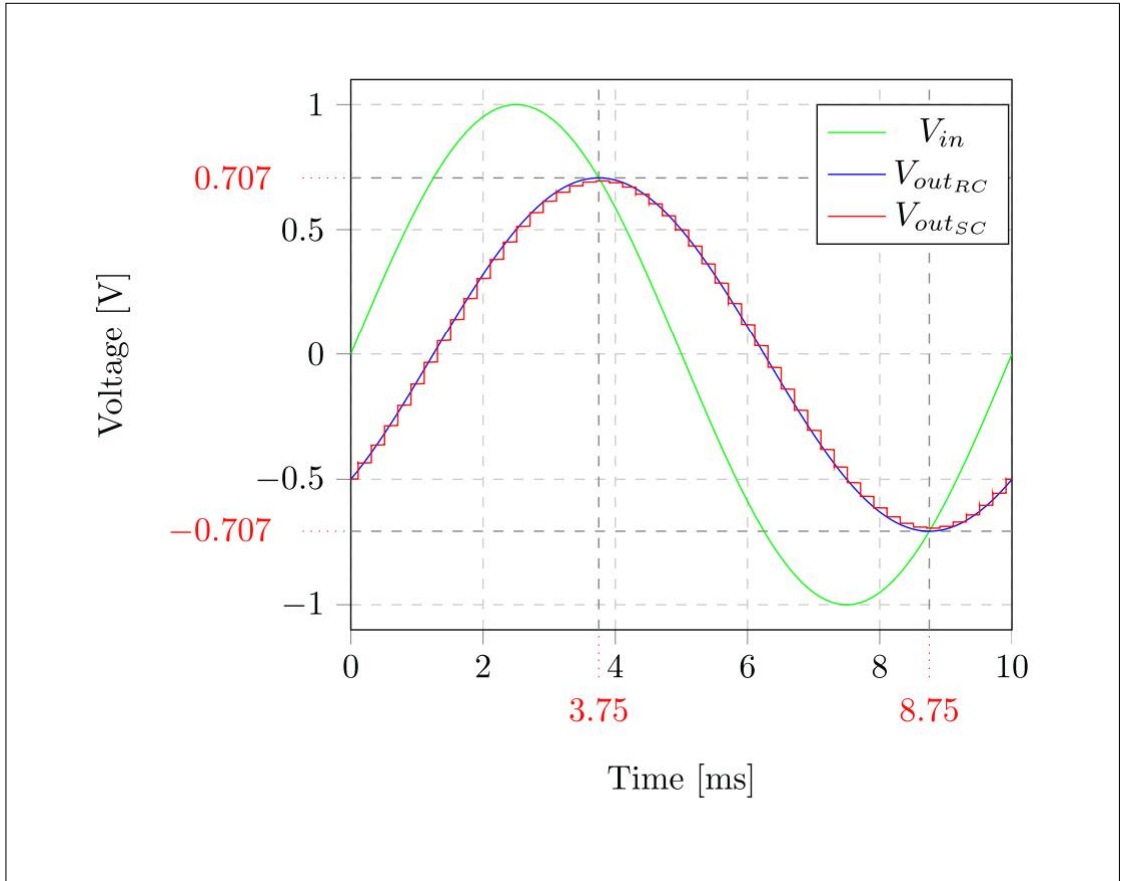


Figure 4.6: Comparison of the output voltages of the First Order RC Low-Pass filter vs Switched-Capacitor Low-Pass filter.

In the following equation, the Switched-Capacitor Low-Pass filter's frequency response is presented.

Definitions:

- $q_L(t)$: Charge on C_L at time "t"
- $q(t)$: Charge on C at time "t"
- $q_L(t - T_{CLK})$: Charge left from the last cycle, computed at $(t - T_{CLK})$

Fundamental Equations:

$q_L(t)$ is a function of both $q(t)$ and $q_L(t - T_{CLK})$. Thus:

- i. $q_{total} = q(t) + q_L(t - T_{CLK})$
- ii. $q_{L_{new}} = q_L(t)$
- iii. $q(t) = C * v_{in}(t)$
- iv. $q_{L_{new}} / C_L = q_{new} / C$
- v. $q_{total} = q_{L_{new}} + q_{new}$ (due to charge conservation)

Derivation:

From (iv):

- $q_{new} = \frac{C}{C_L} q_{L_{new}}$

From (iv), (i), (v) and previous equation:

- $q_{L_{new}} + \frac{C}{C_L} q_{L_{new}} = q_{total} = q(t) + q_L(t - T_{CLK})$
- $\frac{q_{L_{new}}}{C_L} [C_L + C] = C * v_{in}(t) + C_L * v_L * (t - T_{CLK})$
- $v_L(t) = \frac{C}{C + C_L} * v_{in}(t) + \frac{C_L}{C + C_L} * v_L(t - T_{CLK})$

CTFT of the last equation:

- $V_L(j\omega) = \frac{C}{C + C_L} * V_{in}(j\omega) + \frac{C}{C + C_L} * V_L(j\omega) * \exp(-j\omega T_{CLK})$

Therefore:

- $H(j\omega) = \frac{V_L(j\omega)}{V_{in}(j\omega)} = \frac{\frac{C}{C + C_L}}{1 - \frac{C_L}{C + C_L} * \exp(-j\omega T_{CLK})}$

note that if $T_{CLK} \rightarrow 0$ then

- $H(j\omega) = \frac{\frac{C}{C + C_L}}{\frac{C}{C + C_L}} = 1$

as expected.

Using Euler's Identity:

- $$H(j\omega) = \frac{V_L(j\omega)}{V_{in}(j\omega)} = \frac{\frac{C}{C + C_L}}{1 - \frac{C_L}{C + C_L} * (\cos(\omega T_{CLK}) - j * \sin(\omega T_{CLK}))}$$

$$= \frac{\frac{C}{C + C_L}}{1 - \frac{C_L}{C + C_L} * \cos(\omega T_{CLK}) + j * \frac{C_L}{C + C_L} * \sin(\omega T_{CLK})}$$

$$= \left[\frac{\frac{C}{C + C_L}}{1 - \frac{C_L}{C + C_L} * \cos(\omega T_{CLK})} \right] * \left[\frac{1}{1 + j * \frac{\frac{C_L}{C + C_L} * \sin(\omega T_{CLK})}{1 - \frac{C_L}{C + C_L} * \cos(\omega T_{CLK})}} \right]$$

Expand to First-Order Taylor Series:

- $\cos(\omega T_{CLK}) \approx 1$
- $\sin(\omega T_{CLK}) \approx \omega T_{CLK}$

Hence:

$$\bullet H(j\omega) = \frac{\frac{C}{C+C_L}}{\underbrace{1 - \frac{C}{C+C_L}}_1} * \frac{1}{\left[1 + j * \frac{\frac{C_L}{C+C_L} * (\omega T_{CLK})}{1 - \frac{C_L}{C+C_L}} \right]}$$

$$\bullet H(j\omega) = \frac{1}{1 + j\omega * \frac{C_L * T_{CLK}}{C}}$$

Define $f_{CLK} = \frac{1}{T_{CLK}}$ then:

$$\bullet H(j\omega) = \frac{1}{1 + j\omega C_L * \frac{1}{C * f_{CLK}}}$$

Define $R_{eq} = \frac{1}{C * f_{CLK}}$ and $\omega_0 = \frac{1}{C_L * R_{eq}}$:

$$\bullet H(j\omega) = \frac{1}{1 + \frac{j\omega}{\omega_0}}$$

This is equal to First-Order RC Low-Pass Filter's frequency response. The Switched-Capacitor (C) acts like a resistor whose equivalent resistance (R_{eq}) changes in an inversely proportional manner with $f_{CLK} = \frac{1}{T_{CLK}}$ where T_{CLK} is the common clock period of the two switches.

4.4. Switched-Capacitor Integrator

If the feedback resistor of a Negative Feedback Op-Amp circuit is replaced by a capacitor then Op-Amp Integrator circuit presented in figure 4.7 is obtained. The relationship between input and output signals of the Op-Amp Integrator is the mathematical integration operation. In other words, integrator's output signal is the integration of its input signal over the time. This structure has a wide area of usage such as signal generators, ADCs, filters and control circuits. [7],[2]

In the circuit which presented in Figure 4.7 Op-Amp is assumed ideal. In this case **node A** represents a virtual ground and since input resistance of the Ideal Op-Amp is

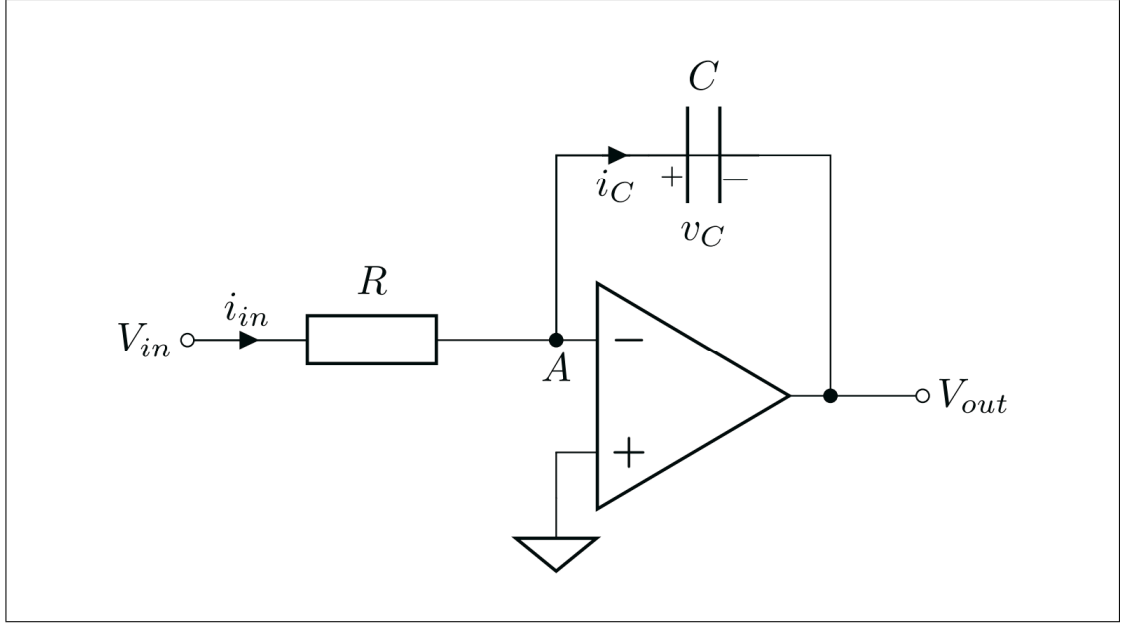


Figure 4.7: Op-Amp RC Integrator circuit.

almost infinite, zero current flows into the Op-Amp's negative input. Thus, assuming the $V_{in} > 0$, source current i_{in} flows through the R and C to the output. Following derivations is presenting Op-Amp Integrator's operation. KCL for node A:

- $i_{in} = \frac{v_{in} - 0}{R} = \frac{v_{in}}{R}$
- $Q = C * v_C$
- $i_C = \frac{dQ}{dt} = C * \frac{dv_C}{dt} = C * \frac{d}{dt}(\underbrace{V_A}_0 - v_{out}) = -C * \frac{dv_{out}}{dt}$

Since we know that $i_{in} = i_C$:

$$\begin{aligned}
 \frac{v_{in}}{R} &= -C * \frac{dv_{out}}{dt} \\
 \frac{dv_{out}}{dt} &= \frac{-1}{RC} * v_{in}(t) \\
 v_{out}(t) &= \frac{-1}{RC} * \int_0^t v_{in}(t) dt
 \end{aligned} \tag{4.8}$$

As presented in above equation integration of input signal is also multiplied by $-\frac{1}{RC}$ either. As known, practical equivalent of the operation of integral is accumulation of the area between the input signal and time axis over the time. Thus, for example,

if a DC voltage level V_{DC} applied to the input of the integrator then output voltage will be a ramp with a slope of $-\frac{V_{DC}}{RC}$ and this continues until output voltage saturates, in other words, reaches to the one of the supply rails of the Op-Amp.

As repeatedly mentioned earlier, in order to adapt circuits into VLSI processes, changing resistors with Switched-Capacitor equivalents is a practical and efficient way. To this end, here, R resistor in the circuit will be replaced by a Switched-Capacitor Resistor which is builded using Transmission Gates. In Figure 4.8, this equivalent circuit is represented. In previous sections, it is proven that Switched-Capacitor Resistor more than adequate for replacing the resistors.

By replacing the R in the Figure 4.7 by Switched-Capacitor Resistor, then Equation 4.8 becomes:

$$v_{out}(t) = -\frac{C_S}{C} f_{CLK} * \int_0^t v_{in}(t) dt \quad (4.9)$$

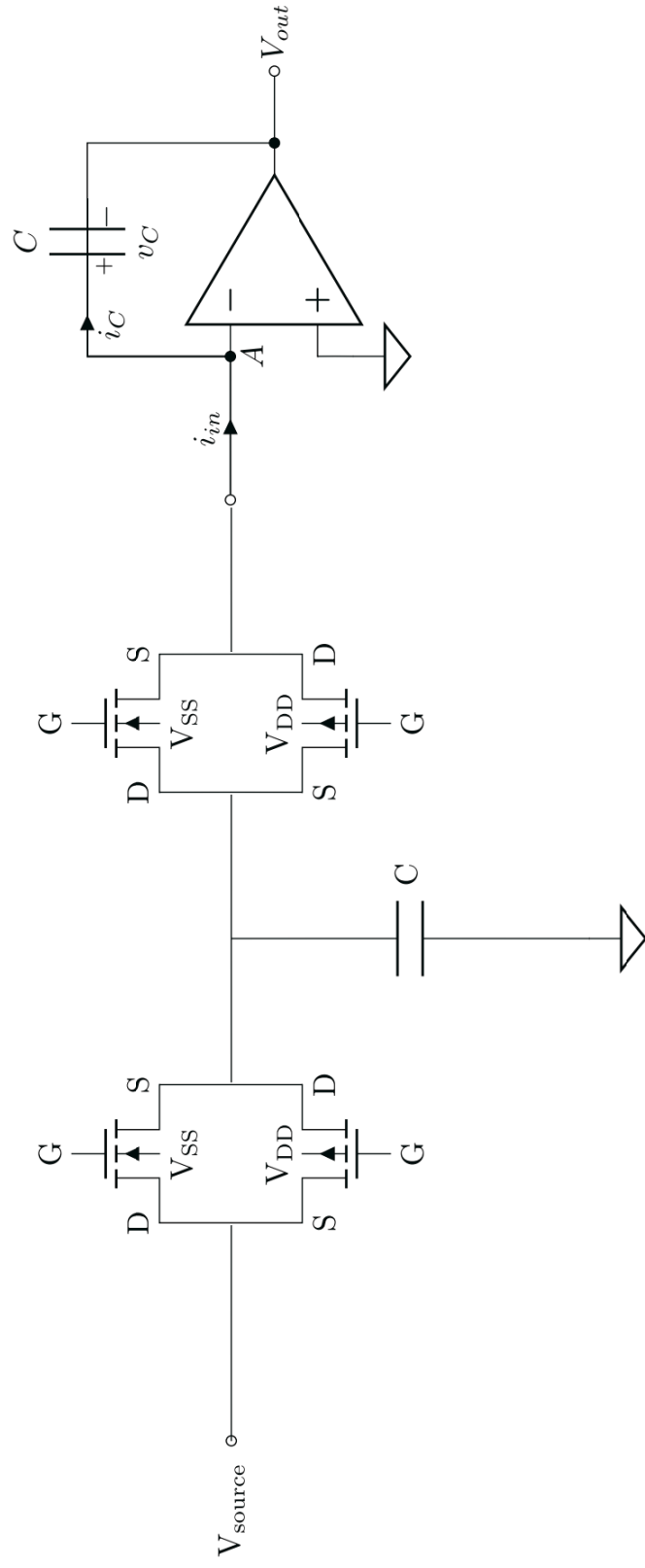


Figure 4.8: Op-Amp Switched-Capacitor Integrator circuit.

In order to show that Switched-Capacitor Resistor comprise of Transmission Gates is performs just like a resistor, an example will be presented. By using the following values presented below, circuits presented in Figure 4.7 and Figure 4.8 are simulated. In this example input voltage is chosen as a sine wave with 0.5V amplitude and 500Hz of frequency.

Table 4.1: Parameters for RC Integrator and Switched-Capacitor Integrator Simulations.

R	$1.59k\Omega$	f_{CLK}	$10kHz$
C	$200nF$	V_{DD}	$1V$
f_{source}	$500Hz$	V_{SS}	$-1V$
$ V_{source} $	$0.5V$	C_S	$62.89nF$

In Figure 4.9 a comparison between source voltage, RC Integrator's output voltage and Switched-Capacitor Integrator's output voltage is presented. As it can be seen in the figure, Switched-Capacitor Integrator's output is almost the same with the RC Integrator's output.

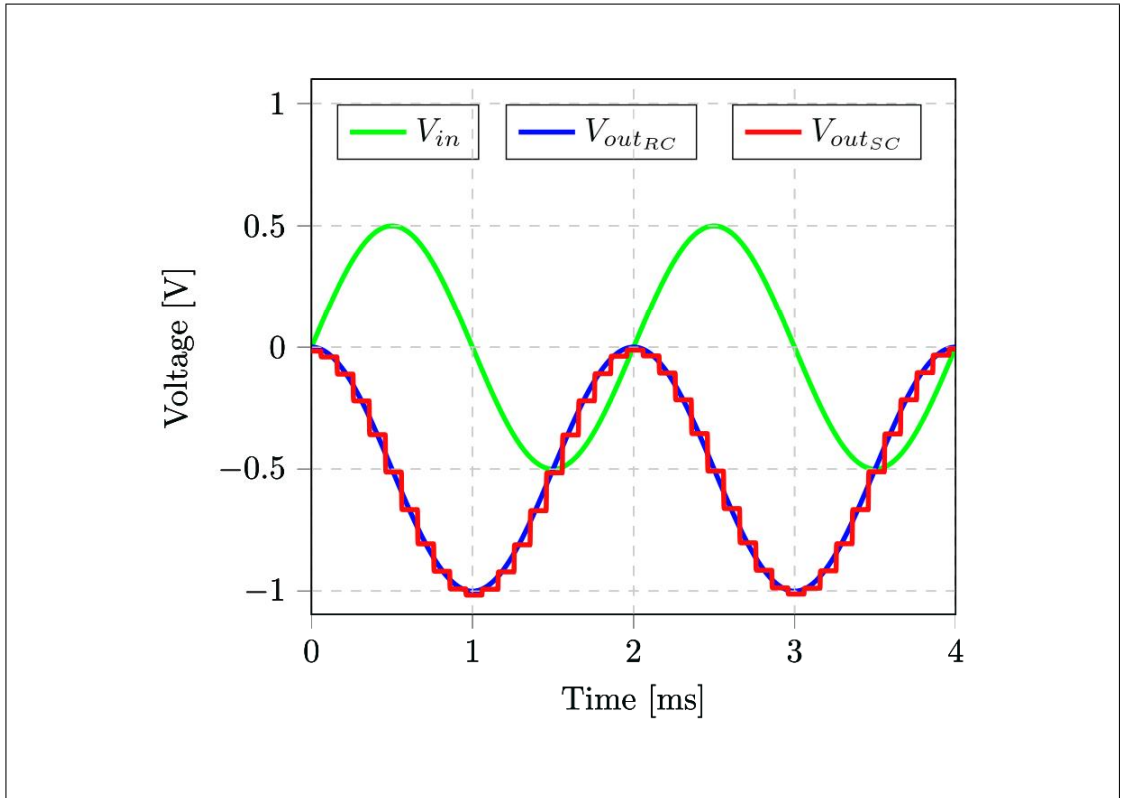


Figure 4.9: Op-Amp Integrator's output voltage vs Switched-Capacitor Integrator's output voltage.

4.5. Switched-Capacitor Common-Mode Feedback

Fully-Differential Amplifiers (FDAs) are widely used in modern signal processing, data transmission and mixed-signal ICs. FDAs are usually preferred in ADC circuits which have differential inputs and outputs. The major difference between FDA and its single-ended counterparts is their differential output stage. FDA has two input and two output terminals which works in a differential fashion. In Figure 4.10, a Fully-Differential Amplifier is presented. [21],[22]

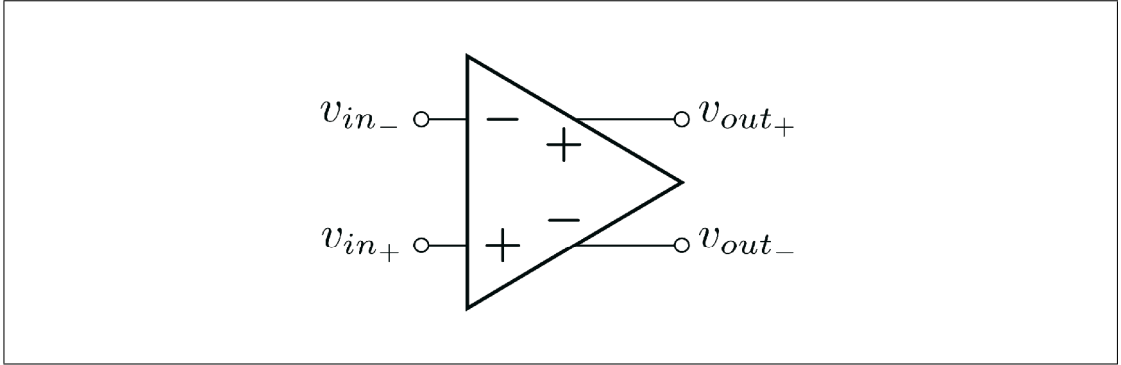


Figure 4.10: Fully-Differential Amplifier.

In an ideal FDA, the voltage difference between the positive and negative output terminals is equal to multiplication of the difference between the input terminals and gain of the FDA. The common voltage at the output is not related with the input voltages and it can be adjusted using another input. In the following equations, input difference voltage (V_{id}), input common voltage (V_{ic}), output difference voltage (V_{od}) and output common voltage (V_{oc}) are presented: [21]

$$V_{id} = V_{in+} - V_{in-} \quad (4.10)$$

$$V_{od} = V_{out+} - V_{out-} \quad (4.11)$$

$$V_{icm} = \frac{V_{in+} + V_{in-}}{2} \quad (4.12)$$

$$V_{ocm} = \frac{V_{out+} + V_{out-}}{2} \quad (4.13)$$

In order to control an Op-Amp's output there must be a feedback circuit from output to input. Since an FDA has two outputs, two feedback circuits can be implemented in order to control differential output voltages. However, output common-voltage is

another parameter which must be controlled. In real applications, some noise originated from other circuit components, medium or power source may be added onto signals which are transmitted by differential transmission lines such as input of the FDA. Those noises usually reveals themselves as common voltages. FDAs inherently immune to these noises because of its differential structure of input, output and supply input terminals. However, in reality, they cannot block all common voltages or noises. In order to control output common-voltage level a feedback circuit called *Common-Mode Feedback(CMFB)* must be implemented. In this chapter a Switched-Capacitor CMFB circuit application will be explained. [22]

There are several configurations used to implement a CMFB circuit. The simplest version of a CMFB is can be made by using resistors and capacitors. Also, in order to make a VLSI compatible CMFB circuit it can be done by using MOSFETs. Those are the CMFB types used in continuous-time circuits. In discrete-time (or sampled data) systems, Switched-Capacitor CMFB circuits are widely used. They offer fast response and versatility.

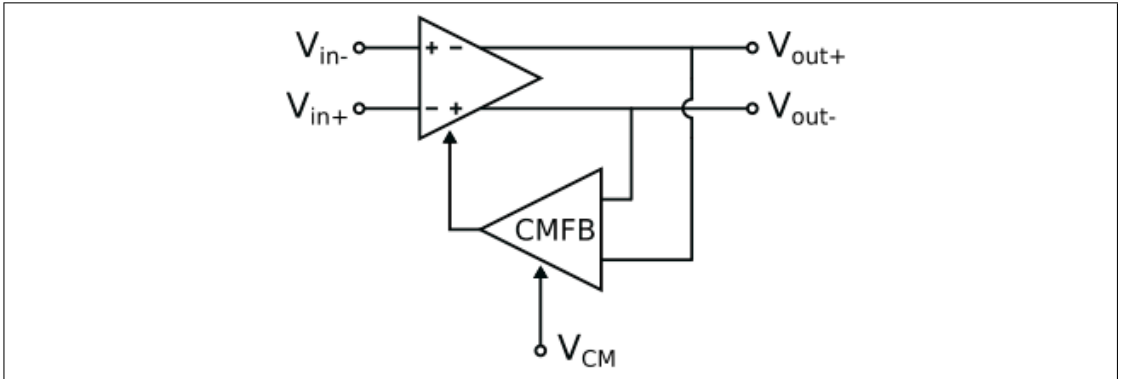


Figure 4.11: Fully-Differential Amplifier and Common-Mode Feedback circuit.

In Figure 4.11, an FDA and its Common-Mode Feedback circuit is presented. This is a simple diagram which demonstrates the operation of this structure. In Figure 4.12, common-mode and differential mode input and output signals are presented. As can be seen in Figure 4.12a, when same signal applied to both inputs, differential output signal or voltage difference between output terminals becomes zero and only voltage level observed on the output is the common voltage. On the other hand, when a differential signal applied to the input terminals as presented in Figure 4.12b, a signal with a larger

amplitude on a common-voltage level can be observed. Here V_{out} represents the voltage difference between the output terminals.

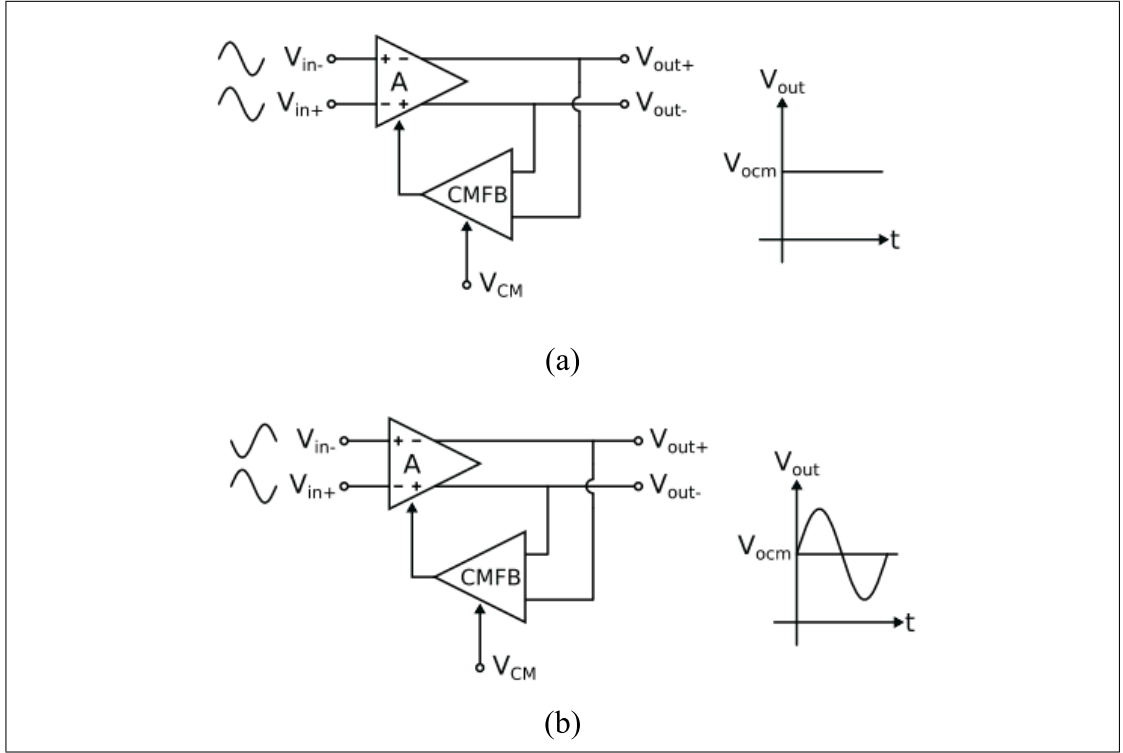


Figure 4.12: a) Common-Mode and b) Differential output signals of an FDA for given inputs.

In Figure 4.13, a Switched-Capacitor Common-Mode Feedback circuit configuration is presented [3], [1]. Here:

- V_{in+} : Voltage level on positive output terminal of the FDA
- V_{in-} : Voltage level on negative output terminal of the FDA
- V_{ref} : Common-Voltage reference value provided by FDA
- V_{ocrm+} : Voltage level on positive output terminal of the CMFB
- V_{ocrm-} : Voltage level on negative output terminal of the CMFB
- V_{ocrm} : Common-Voltage feedback of CMFB

This circuit operates based on charge transfer between capacitors. At ϕ_1 , the first switches become ON and charge on the C_1 capacitors is shared between C_1 and

C_2 capacitors. Thus, voltage on C_1 capacitors are applied on C_2 either. At ϕ_2 , first switches turns off and second switches turns on. At this point voltage drop on the C_2 capacitors and C_o capacitors becomes equal. Thus, voltage applied to the input terminals of the CMFB is carried to output terminals.

In a practical manner, input common-voltage (V_{icm}), which is expressed in Equation 4.12, can be defined as a DC voltage level which exist in both input signals and V_{ref} represents the desired input common voltage level. CMFB circuit's function is to determine the voltage difference between the existing common voltage level and desired common voltage level and produce an error signal which is equal to:

$$V_{ocm} = V_{ref} - V_{icm} \quad (4.14)$$

Thus error amplifier in the FDA can use this signal and adjust the common voltage level to the desired value.

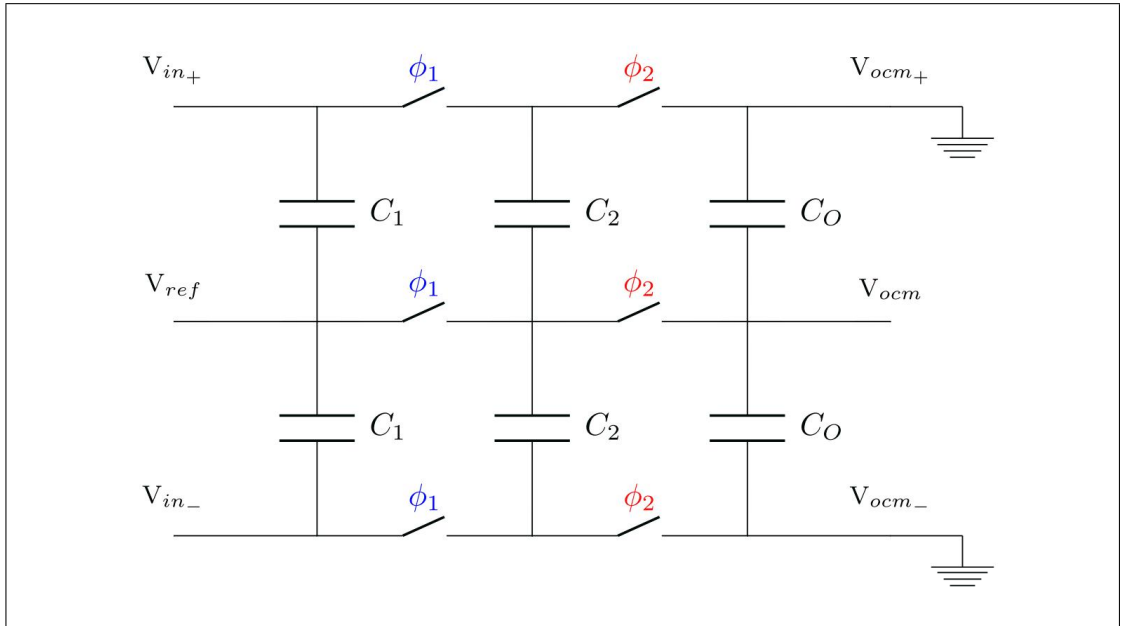


Figure 4.13: Switched-Capacitor CMFB circuit using ideal SPST switches.

In Figure 4.14, Switched-Capacitor CMFB circuit comprised of Transmission Gates is presented. In order to visualize the explanations took place in this chapter a simulation of this circuit will be made. Thus, consistency of the Transmission Gates and

Switched-Capacitor CMFB circuit will be showed and a better understanding about the subject will be provided.

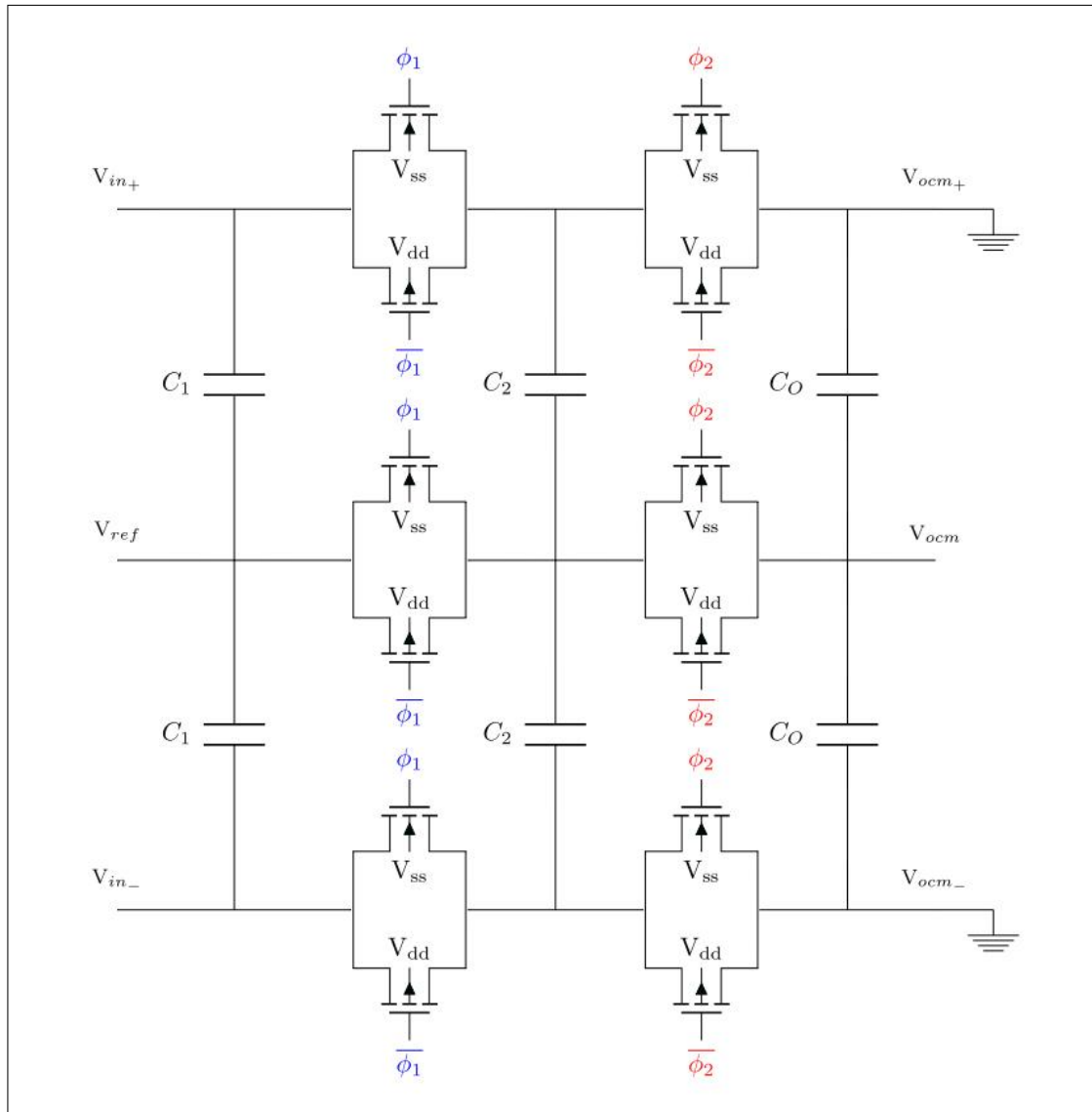


Figure 4.14: Switched-Capacitor CMFB circuit using Transmission Gates.

In Figure 4.15, differential input signals, and as a function of these, input common voltage is presented. Since the Switched-Capacitor CMFB presented in this study does not include an error amplifier, common voltage level of the input does not change as can be seen in Figure 4.15. This configuration is presented in order to show its capability of producing the feedback signal only.

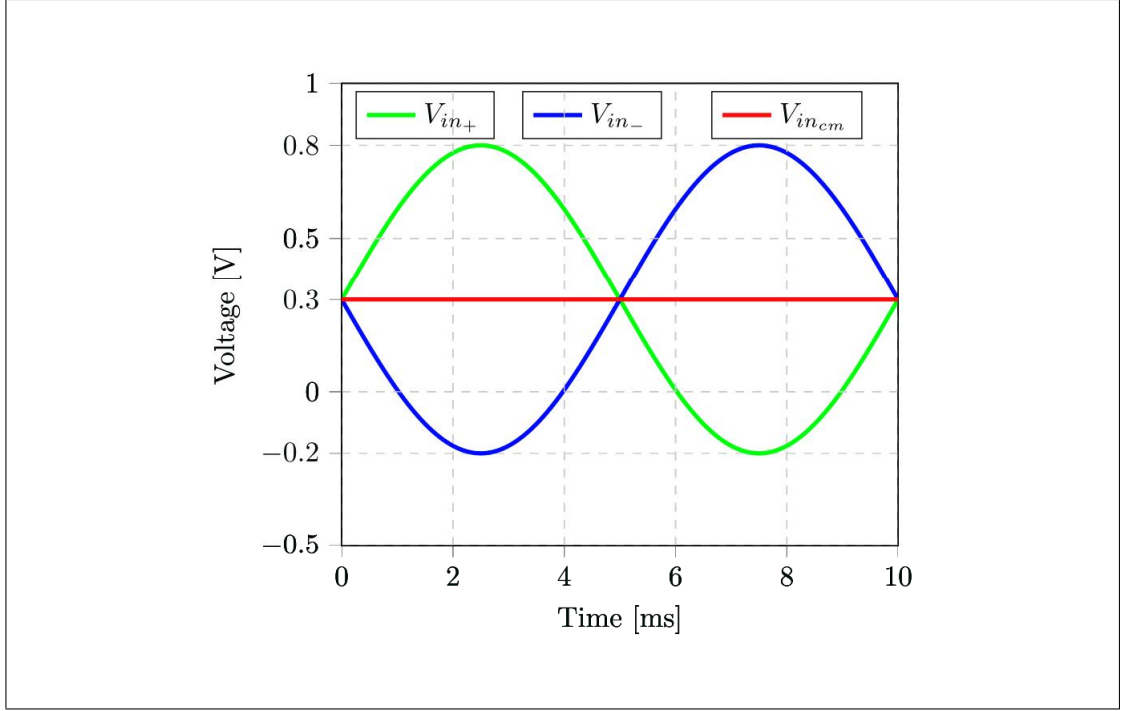


Figure 4.15: Input signals of the Switched-Capacitor CMFB circuit using Transmission Gates.

In Figure 4.16, simulation results of the circuit in Figure 4.14 is presented. In the simulation, a periodically changing input reference voltage applied in order to show CMFB circuit's capability of fast settling and short reaction time.

At the top plot pane in Figure 4.16, periodically changing V_{ref} is presented. In the second pane from the top, input common voltage level is presented. At the third pane, the difference between the reference voltage and the input common voltage is presented as expressed in Equation 4.14. At the last pane, output common voltage is presented. As can be seen in this plots, output common voltage is reacting very fast against the changes occurring in the reference voltage and settling in a very short amount of time.

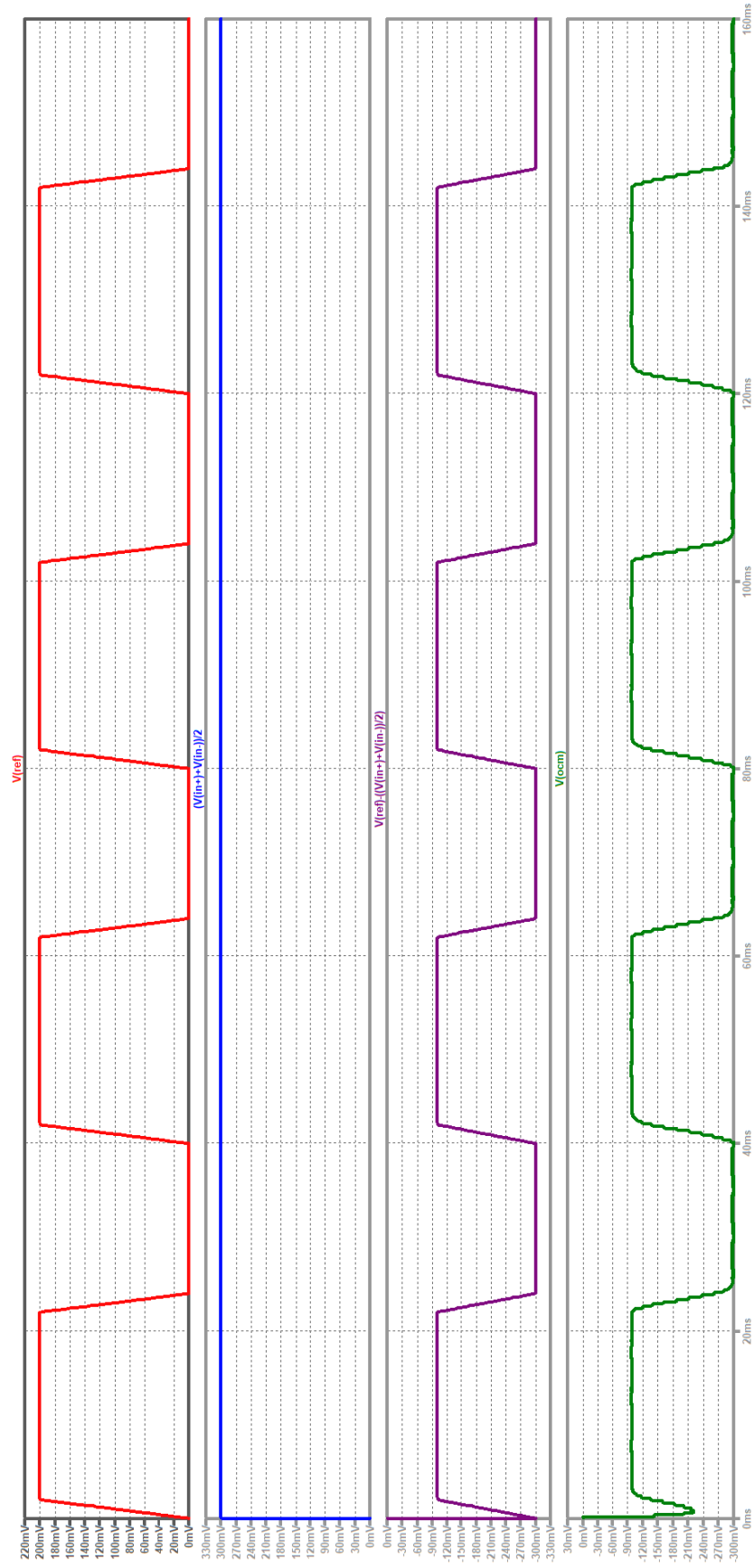


Figure 4.16: Input and Output common mode voltages of the Switched-Capacitor CMFB circuit.

5. CONCLUSIONS

In this master's thesis, Switched-Capacitor Circuits and Applications are studied. Physical structures of the MOSFET switches, which are the building blocks of the switched-capacitor circuits, are examined and their passing performances are compared. Also, parameter values what are needed in order to use MOSFETs as switches are explained. Afterwards, switched-capacitor applications, which are constructed using MOSFET switches, are presented. Performance comparison of these structures are visualized by comparing the simulation outputs of the fundamental circuits with simulation outputs of the switched-capacitor circuits.

In this study, LTspice and ngspice software were used as simulation environment and ASU PTM MOSFET Spice models were used as MOSFET models. Thus, it has been accomplished to create situations closer to real applications. It was presented that the analysis and the equations obtained here were consistent with the simulation outputs.

The parameters of the simulated circuits are specially selected for each application. Minor differences, especially due to the neglect of some disturbing effects seen inherently in MOSFETs, have been minimized by empirically adjusting the parameters of the circuits.

Since Switched-Capacitor Circuits are an active topic that has been studied with increasing interest for many years, each title examined in this thesis can be studied on its own. The applications presented here can be implemented with higher accuracy and closer to real world applications using software with better capabilities and practically tried Spice models.

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BIOGRAPHY

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APPENDICES

Other Appendices (CD)