T.R.
GEBZE TECHNICAL UNIVERSITY
INSTITUTE OF NANOTECHNOLOGY

FABRICATION AND CHARACTERIZATION OF a-Si:H BASED TOP-GATE AND BOTTOM-GATE THIN-FILM TRANSISTORS (TFTs)

ELÇİN MERT
A THESIS SUBMITTED FOR THE DEGREE OF
MASTER OF SCIENCE
DEPARTMENT OF
NANOSCIENCE AND NANOENGINEERING

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a-Si:H TABANLI ÜST-KAPI VE ALT-KAPI İNCE FİLM TRANSİSTÖRLERİN (TFTs) FABRİKASYONU VE KARAKTERİZASYONU

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NANOBİLİM VE NANOMÜHENDİSLİK
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GEBZE
2019

GEBZE TEKNİK ÜNİVERSİTESİ	**YÜKSEK LİSANS JÜRİ ONAY FORMU**

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SUMMARY

Hydrogenated amorphous silicon thin-film transistors are widely used devices for large-area electronics applications such as flat panel displays, medical imagers, and sensors. Especially the backplanes of active-matrix LCDs and active-matrix OLEDs are based on TFTs comprising a-Si:H active layers using as switching and driving devices. a-Si:H is the material of choice for large area electronics and leading in the flat panel display industry due to its possibility of uniform deposition over large areas, low deposition temperatures, standard fabrication process, and low costs.

a-Si:H based TFTs are metal-insulator-semiconductor field effect transistors (MISFETs) which include three device layers to operate: a gate metal, a gate dielectric, and a semiconductor active layer. In this study, Cr, SiN_x/Al_2O_3 (bilayer gate dielectric structure), and a-Si:H were used as gate metal, gate dielectric, and active channel layer material, respectively. The following microfabrication techniques are used for fabricating a-Si:H based TFT devices in top-gate and bottom-gate configurations: photolithography, PECVD (for amorphous silicon and silicon nitride depositions), ALD (for alumina deposition), DC magnetron sputtering (for metal depositions), wet etching, and ICP-RIE as a dry etching.

The aim of this study is to develop a-Si:H based TFT devices for large area electronics, especially AMOLED applications. In accordance with this purpose, we have successfully fabricated TFT devices with top-gate and bottom-gate architectures. The I_d-V_{ds} characteristics of TFTs were obtained and studied. Field effect mobility of approximately 0.08 $cm^2V^{-1}s^{-1}$ was obtained from some of the devices. As a result of the study, these TFTs proved to be used in AMOLED applications.

Keywords: Thin-Film Transistors (TFTs), Microfabrication, Photolithography, Hydrogenated Amorphous Silicon (a-Si:H), Top-Gate TFT, Bottom-Gate TFT.

ÖZET

Hidrojene amorf silikon ince film transistörler düz panel ekranlar, tıbbi görüntüleme cihazları ve sensörler gibi geniş alan elektronik uygulamalarında yaygın olarak kullanılmaktadırlar. Özellikle aktif-matris LCD ve aktif-matris OLED ekranların arka-planları anahtarlama ve sürücü elemanlar olarak kullanılan a-Si:H aktif katmanlarını içeren TFT'lere dayanmaktadır. Geniş alanlar üzerinde uniform depozisyon, düşük depozisyon sıcaklıkları, standart fabrikasyon süreci ve düşük maliyet nedenlerinden dolayı a-Si:H geniş alan elektroniği için tercih edilen ve düz panel ekran endüstrisinde lider bir malzemedir.

a-Si:H tabanlı TFT'ler metal-yalıtkan-yarı iletken alan etkili transistörlerdir (MISFET) ve dolayısıyla yapısında kapı metali, kapı dielektriği ve yarı iletken aktif katmanlarını içerirler. Bu çalışmada, Cr, SiN_x/Al_2O_3 (iki katmanlı kapı dielektriği yapısı) ve a-Si:H sırasıyla kapı metali, kapı dielektriği ve aktif kanal katmanı malzemesi olarak kullanılmıştır. Üst-kapı ve alt-kapı konfigürasyonlarında a-Si:H tabanlı TFT aygıtlarının üretilmesi için kullanılan mikrofabrikasyon teknikleri şunlardır: fotolitografi, PECVD (amorf silikon ve silikon nitrat depozisyonları için), ALD (alümina depozisyonu için), DC magnetron sıçratma tekniği (metal depozisyonları için), ıslak aşındırma ve kuru aşındırma olarak ICP-RIE sistemi.

Bu çalışmanın amacı, geniş alan elektroniği için, özellikle AMOLED uygulamaları için a-Si:H tabanlı TFT aygıtları geliştirmektir. Bu amaç doğrultusunda, üst-kapı ve alt-kapı mimarilerinde TFT aygıtlarının fabrikasyonları başarıyla gerçekleştirilmiştir. TFT'lerin I_d-V_{ds} karakteristikleri elde edilmiş ve çalışılmıştır. Bazı aygıtlardan yaklaşık 0.08 $cm^2V^{-1}s^{-1}$ alan etkisi mobilitesi elde edilmiştir. Çalışma sonucunda, bu TFT'lerin AMOLED uygulamalarında kullanılabilirlikleri kanıtlanmıştır.

Anahtar Kelimeler: İnce Film Transistörler (TFTs), Mikrofabrikasyon, Fotolitografi, Hidrojene Amorf Silikon (a-Si:H), Üst-Kapı TFT, Alt-Kapı TFT.

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LIST of ABBREVIATIONS and ACRONYMS

Symbols and Abbreviations	**Descriptions**
Å	: Angstrom
C_{ox}	: Capacitance of Gate
L	: Channel Length
λ	: Channel Length Modulation Parameter
W	: Channel Width
Cr	: Chromium
c-Si	: Crystalline Silicon
I_d	: Drain Current
V_{ds}	: Drain-Source Voltage
V_A	: Early Voltage
eV	: Electron Volt
V_{gs}	: Gate-Source Voltage
a-Si:H	: Hydrogenated Amorphous Silicon
K	: Kelvin
MHz	: Megahertz
μc-Si	: Microcrystalline Silicon
mJ	: Millijoule
μ	: Mobility of Electrons
nc-Si	: Nanocrystalline Silicon
nm	: Nanometer
Ω	: Ohm
poly-Si	: Polycrystalline Silicon
V_t	: Threshold Voltage
g_m	: Transconductance
Vs	: Volt Second
AMFPD	: Active Matrix Flat Panel Display
AMLCD	: Active Matrix Liquid Crystal Display
AMOLED	: Active Matrix Organic Light Emitting Diode

ALD	: Atomic Layer Deposition
BJT	: Bipolar Junction Transistor
BG	: Bottom Gate
CAGR	: Compound Annual Growth Rate
DI	: Deionized Water
DOS	: Density of States
DC	: Direct Current
FET	: Field Effect Transistor
HMDS	: Hexamethyldisilazane
ICP-RIE	: Inductively Coupled Plasma - Reactive Ion Etching
IPA	: Isopropyl Alcohol
MISFET	: Metal Insulator Semiconductor Field Effect Transistor
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
PECVD	: Plasma Enhanced Chemical Vapor Deposition
RF	: Radio Frequency
rpm	: Revolutions Per Minute
SCS	: Semiconductor Characterization System
TFT	: Thin Film Transistor
TG	: Top Gate
UHV	: Ultra High Vacuum
UV	: Ultra Violet

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1. INTRODUCTION

Studies about amorphous semiconductors were first carried out in the 1950s and 1960s. Researches especially include structural disorder in amorphous semiconductor materials and influence of disorder on the electronic properties of amorphous semiconductors. Amorphous silicon (a-Si) without hydrogen deposited by using PVD techniques such as sputtering or thermal evaporation was used as a semiconductor material in the experimental studies. Non-hydrogenated amorphous silicon has very high electronic defects because of the dangling bonds in its structure. The high defect density in a-Si prevented the desirable characteristics such as doping, photoconductivity, etc. of a good semiconductor material. In 1969, Chittick et al. made the first hydrogenated amorphous silicon (a-Si:H) from the silane (SiH_4) plasma which was prepared by glow discharge deposition technique [1]. So, the defect states in a-Si were reduced considerably by using hydrogen passivation of dangling bonds. Figure 1.1 shows the schematic representation of the atomic structures of crystalline silicon and a-Si:H [2].

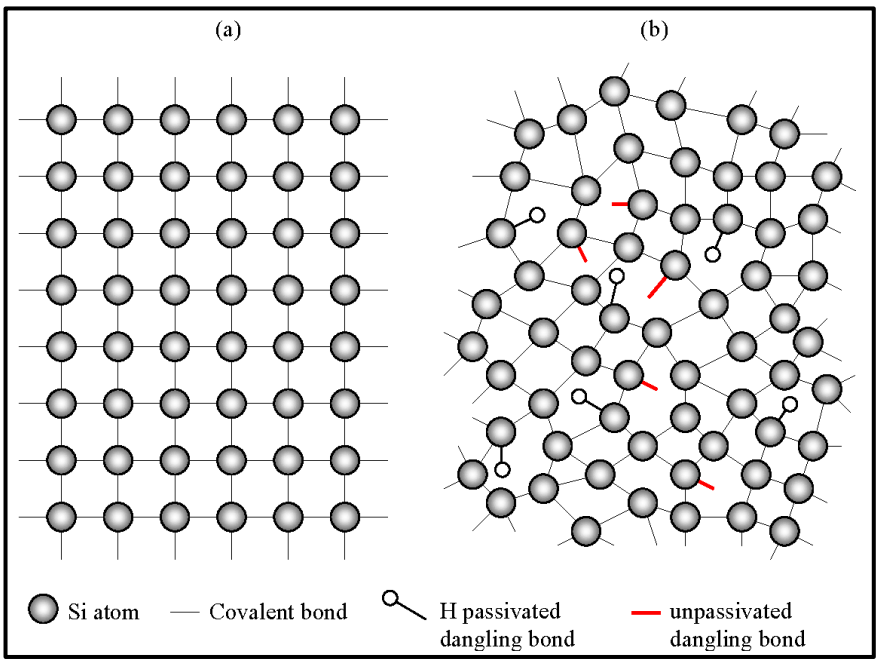

Figure 1.1: Model for the atomic structure of (a) single crystal silicon (b) hydrogenated amorphous silicon.

A few years later, the research of Spear et al. showed that the a-Si:H had good electrical transport properties due to the its very low defect density which include the quite high carrier mobility and strong photoconductivity [3]. The bonding disorder significantly influences the electronic properties of the material and also the design of the a-Si:H devices. Some important characteristic parameters for good electronic quality a-Si:H are listed in Table 1.1 [4].

Table 1.1: Some of the fundamental electronic parameters of a-Si:H (according to the details of the deposition conditions, the exact values can change).

Electron drift mobility	1 cm^2/Vs
Hole drift mobility	0.003 cm^2/Vs
Optical band gap	1.7 eV
300 K conductivity (undoped)	10^{-11} $\Omega^{-1}cm^{-1}$
300 K conductivity (n^+)	10^{-2} $\Omega^{-1}cm^{-1}$
300 K conductivity (p^+)	10^{-3} $\Omega^{-1}cm^{-1}$
Defect density	10^{-15} cm^{-1}
Diffusion length	3000 Å
Hydrogen concentration	10 at. %

During the development process of a-Si:H, another major point was the discovery of substitutional doping in 1975 [5]. N-type or p-type doped a-Si:H was obtained by the addition of phosphine (PH_3) or diborane (B_2H_6) to the silane plasma during the deposition. Then, the first a-Si:H p-n junction was invented in 1976 [6]. The developments in the photovoltaic material and device technology caused to start of research works about a-Si:H device. And mainly with the discovery of doping, in 1976, Carlson and Wronski showed the applicability of a-Si:H solar cells with 2-3 % as initial efficiencies [7]. Then, in 1979, LeComber et al. made the first a-Si:H thin film transistor (TFT) which included the plasma deposited silicon nitride as gate dielectric layer. The first a-Si:H TFT structure and transfer characteristics are shown in Figure 1.2 [8].

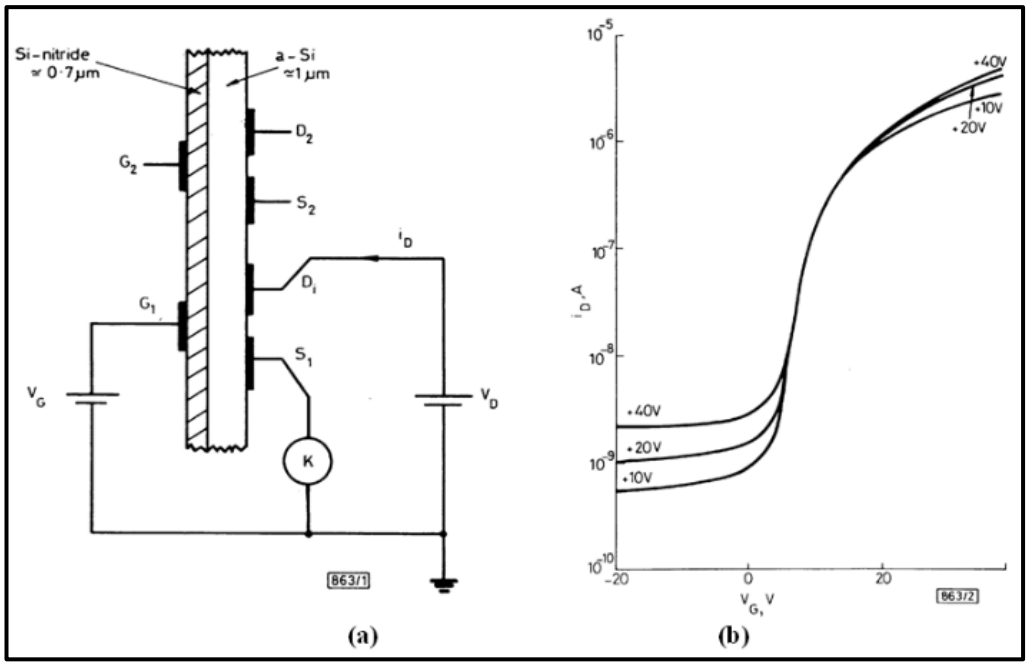

Figure 1.2: The (a) structure and (b) transfer characteristics of the first a-Si:H TFT.

The plasma nitride was a critical development which provided that these TFTs were fabricated on a glass substrate at low process temperatures with high on/off current ratio. Finally, a few years after the first field effect transistors were reported, Snell et al. demonstrated large area electronic arrays of a-Si:H devices [9]. These devices benefit from the capability to deposit and process a-Si:H over large areas. Since that date, many applications such as liquid crystal displays, optical scanners, and radiation imagers are based on a-Si:H TFT technology. The a-Si:H TFT appeared as the best solution to the fabrication of matrix addressed arrays for optoelectronic applications.

1.1. Material Properties and Device Applications of Amorphous Silicon

Hydrogenated amorphous silicon has demonstrated to be the preferred semiconductor material for use as active layer in large area electronic devices for some fundamental reasons. Firstly, amorphous silicon is a good material that includes all the useful properties of a semiconductor such as doping, junction formation, photoconductivity, field-effect modulation of conductivity, etc. Because of the similarity of chemical and atomic structure to crystalline silicon (c-Si),

amorphous silicon device fabrication can benefit from the extensive knowledge for crystalline-silicon-based processing developed through the microelectronics industry. Since some of fabrication processes of a-Si:H is like those of c-Si, certain equipments used in standard c-Si processes can easily be re-scaled for a-Si:H processes. Therefore, these standard fabrication processes reduce capital costs. The plasma-enhanced chemical vapor deposition (PECVD) technique allows for low cost and uniform growth of a-Si:H material over large areas. And also, the PECVD process used to deposit amorphous silicon can be easily applied to the growth of a diverse set of alloy materials which provide dielectrics, passivation layers and semiconductors with different bandgaps needed for electronic device applications. For these reasons, a-Si:H technology is attractive in large area applications. Some applications are displays [10], scanners [11], position sensors [12], medical imagers [13], and solar cells [14]. The most popular applications of a-Si:H technology are liquid crystal displays and, most recently, organic light emitting diode displays.

1.2. Motivation

Large-area electronics is fastly growing and expanding field expected to affect all aspects of human life such as energy, health and environment. Large area applications contain but are not limited to switching and driving elements for active matrix flat panel displays (AMFPDs) based on liquid crystal pixels (AMLCDs) and organic light emitting diodes (AMOLEDs), medical imagers, pressure sensors, low-power communication and energy harvesting are shown in Figure 1.3 [15, 16].

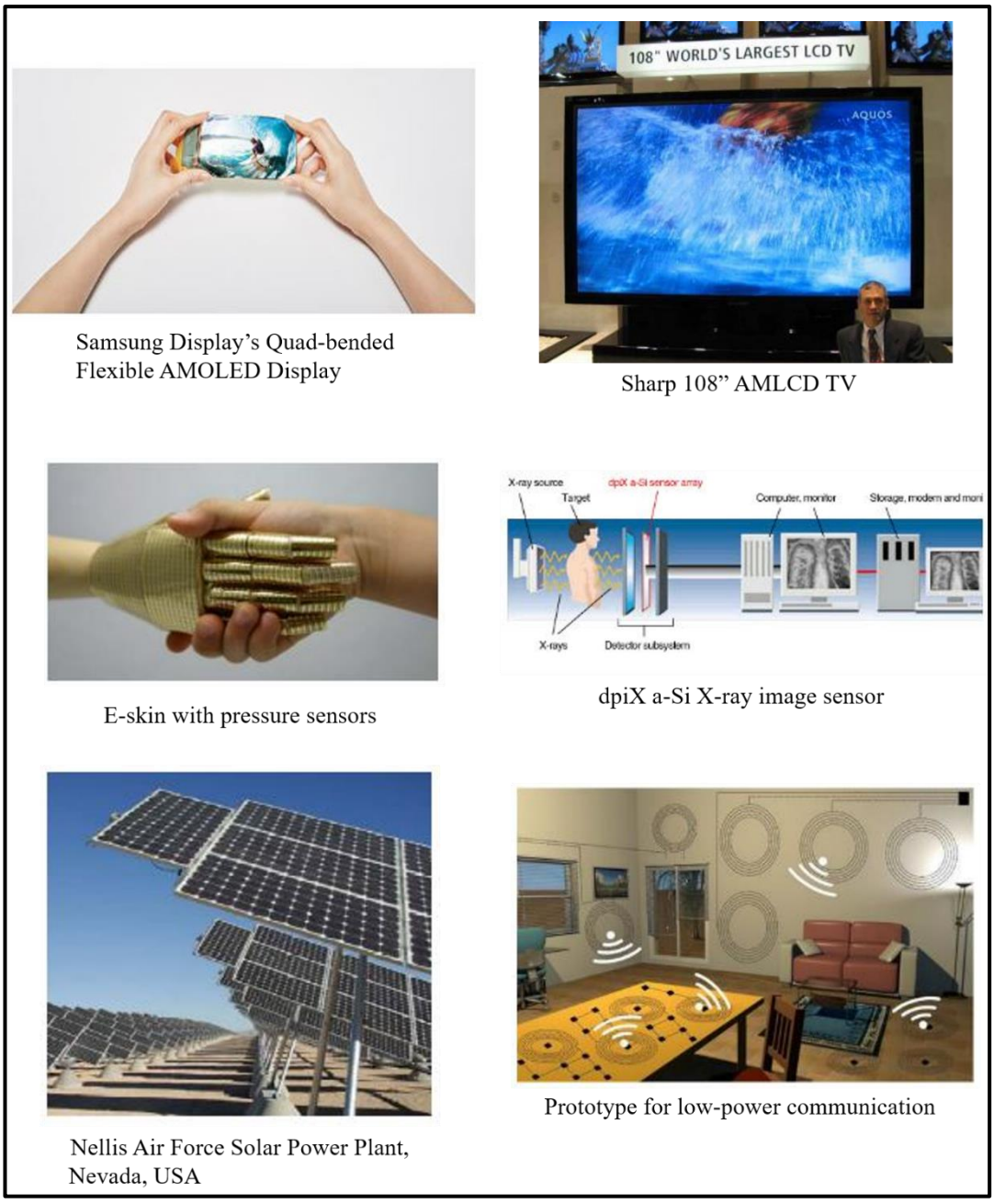

Figure 1.3: Different large area applications of a-Si:H TFT such as AMLCD, AMOLED, medical imager, pressure sensor, low-power communication and energy harvesting (the Samsung AMOLED Display won the 2017 award about ‘‘Displays of the Year’’ of the Society for Information Display, SID).

In large area electronics, the flat panel display industry is the largest industry. In a report titled ‘‘Flat Panel Display Market: Global Industry Analysis & Opportunity Assessment 2017–2027’’, Future Market Insights presents a revised forecast of the global flat panel display market for a 10-year forecast period from 2017 to 2027. The global flat panel display market is anticipated to grow from US$

152.928 Mn in 2017 to US$ 177.339 Mn by 2027, expanding at a CAGR of 4.4% in terms of revenue during the forecast period (2017–2027). In the past quarter-century, thin film transistors have become the “backbone” of the electronic flat panel industry, just like silicon chips were previously the “backbone” of the electronic computer revolution [17]. In particular, the increasing demand for consumer electronic devices and the expanding economies of the world are key factors driving growth in the global market for thin film transistors. In a report, Thin Film Transistors: Global Markets to 2022, BCC Research estimates this market will reach $230.0 Million by 2022 from $105.0 Million in 2017, indicating a compound annual growth rate (CAGR) of 17.0%. The fixed technology in large area electronics applications, especially the backplanes of active matrix displays, is currently based on TFTs with hydrogenated amorphous silicon active layers [18]. The rapid advancements in technology, encourage the invention of better and cost-effective technologies. The active-matrix organic light-emitting diode is one of today’s most energy-efficient and rapidly developing technologies. The AMOLED Display market is expected to grow at approximately USD 14 Billion by 2023, at 18% of CAGR between 2017 and 2023 (Figure 1.4).

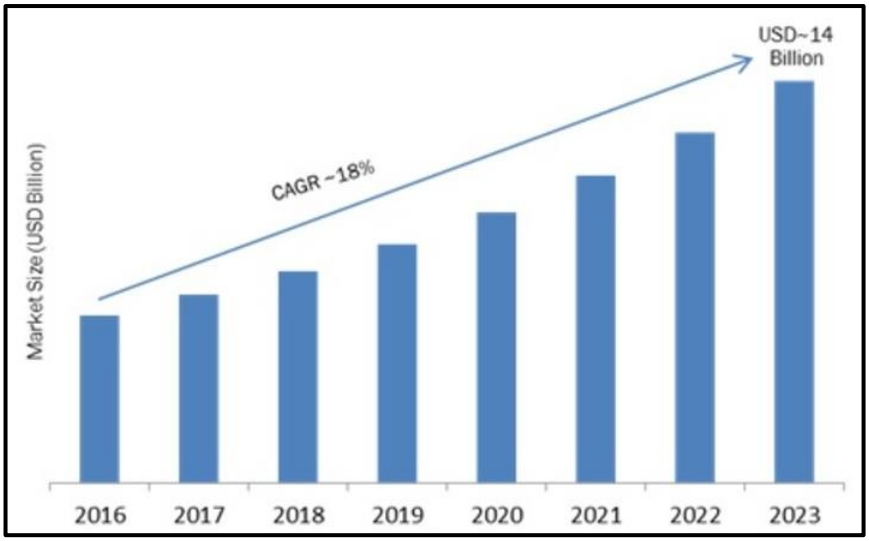

Figure 1.4: AMOLED Display Market. Adapted from Market Research Future.

In addition, TFT LCDs today represent one of the most popular technologies in the display industry. According to a report by Expert Market Research, the global TFT LCD market reached a value of US$ 138 Billion in 2016 and is further expected to reach US$ 193 Billion by 2022. On the other hand, other TFT technologies like

polycrystalline silicon (poly-Si), microcrystalline silicon (μc-Si), organic semiconductors and metal oxides draw the attention of researchers as the applications for large-area electronics expand. Table 1.2 summarizes the comparison of different TFT technologies briefly [19, 20].

Table 1.2: Different TFT technologies.

Attribute	**a-Si**	**μc-Si**	**poly-Si**	**Organic**	**Metal oxides**
Circuit type	NMOS	NMOS/PMOS	NMOS/PMOS	PMOS	NMOS
Mobility	low	higher than a-Si	high	low	high
Stability	issue	stable	stable	issue	under investigation
Uniformity	high	potentially high	improving	improving	high
Manufacturability	mature	RF PECVD?	new	has potential	has potential
Cost	low	low	high	potentially low	low
Flexible substrate	promising	promising	uncertain	promising	promising

Based on different TFT technologies, including a-Si TFT, new functions or applications of TFTs have been reported apart from display applications. For instance, using the floating-gate structure, the a-Si:H TFT has been made into a nonvolatile memory device [21]. Furthermore, TFT-based chemical, electrical, optical, biological, and magnetic sensors or detectors made by changing the transistor structures, composition of the thin films, attached devices, etc. are given in Table 1.3 [22].

Table 1.3: Various applications of different TFTs-based in non-display applications.

TFT Area	Functions	Principles of operation
Gate dielectric	pH sensing	H^+ adsorption in suspended gate dielectric structure
	Memory	PZT gate dielectric
Semiconductor	Gas sensing	H_2O, alcohols, N_2O adsorption on semiconductor layer
	IR detection	I_d = f(temperature)
Gate electrode	Gas sensing	H_2 decomposition on Pd gate electrode
	Bio sensing	Biomolecule reaction with agents on gate electrode
S/D electrodes	Protein/DNA analysis	Contact resistance change due to biomolecule adsorption
	Artificial retina	Photoconductivity change on attached a-Si:H layer
	X-ray imaging	Scintillator light emission on attached diode
	LEDs	Quantum dot light emission
Structures	Photo sensing	I_{light}/I_{dark} ratio enhanced by split or offset gate
	Memory	Floating-gate dielectric
	Magnetic	Hall effects due to additional electrodes

Different device performance standards are needed for different large-area applications, but the general principles for the requirements of TFTs in large area electronics are low processing temperature (~300ºC for glass substrates, ~350ºC for metal foil substrates and ~150ºC for plastic substrates), low leakage current, high on/off ratio, low voltage operation, small area, high uniformity and high stability. So, all these requirements are always important for the commercialization of a TFT to be fabricated.

1.3. Organization of the Thesis

This thesis reports the fabrication and characterization of the hydrogenated amorphous silicon TFTs.

Chapter 2 provides a required fundamental theoretical background to understand such devices. Firstly, brief information is given about the physics of amorphous silicon, which is the semiconductor material of the devices. TFTs are similar to conventional silicon MOSFETs in terms of composing layers and operation. Therefore, the basic operation principles of these devices are reviewed, separately. Also, an overview of TFT is provided with its configurations and materials.

Chapter 3 consists of a detailed description of the fabrication methods and equipment used in this thesis. The fabrication process is examined under two main subtopics as thin film deposition and thin film patterning. In addition, this chapter includes briefly the used electrical characterization equipment and method that is used to analyze the device characteristics.

Chapter 4 includes the fabrication steps and details of a-Si:H based thin-film transistors, and presents the electrical characterization results of the fabricated devices.

Chapter 5 concludes the thesis by making a brief summary of this study and the possible future research to be ignited by the findings of this thesis.

2. THEORETICAL BACKGROUND

2.1. Density of States

c-Si materials are defined with conduction band edge, valance band edge and the band gap because of that these materials possess long range order in its periodic lattice structure. The density of states (DOS) distribution of c-Si is illustrated in Figure 2.1 [23]. No defect states are assumed to exist in the forbidden region in DOS distribution of c-Si. Also, valance and conduction band edges are abrupt.

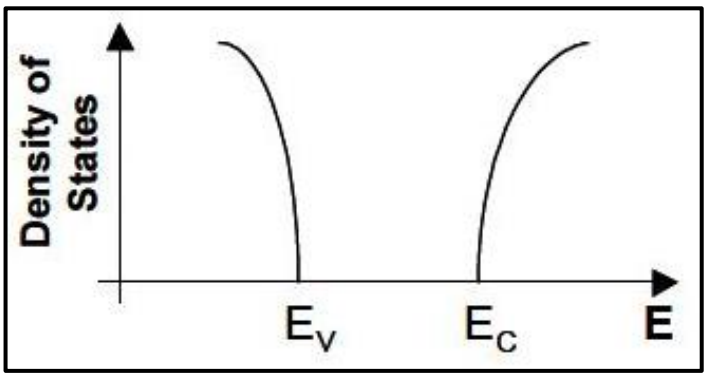

Figure 2.1: DOS distribution in crystalline silicon.

On the other hand, for a-Si materials, they retain short range order characteristics of Si lattice, because these materials do not possess long range order. In comparison with c-Si, a-Si has a complex DOS distribution due to that it includes high density of dangling bond defects. In DOS distribution of a-Si as shown in Figure 2.2, it has conduction and valance bands just like c-Si, but the band tails of a-Si are extended into the forbidden gap [23, 24]. These tail states result from variation in bond lengths and angles in the structure of a-Si. In addition to this, there are also deep states in a-Si. Dangling bonds and other microscopic point defects create these deep states [25].

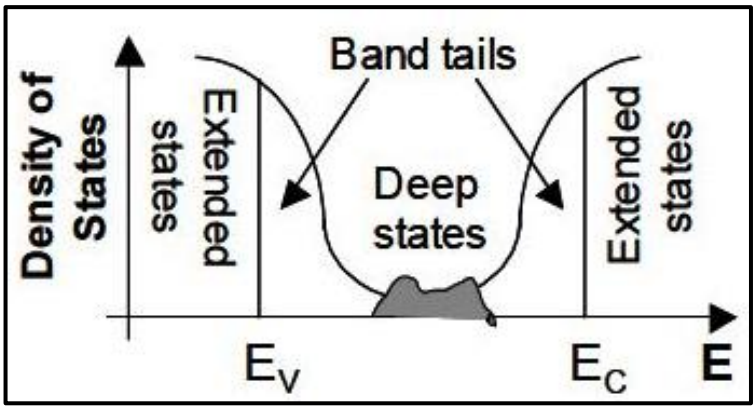

Figure 2.2: DOS distribution in amorphous silicon.

As shown in Figure 2.2, the tail states near the conduction band having a narrower distribution than the tail states near the valance band, so the DOS distribution of a-Si in the mobility gap is asymmetrical. This asymmetry means more holes have been trapped resulting in a lower hole mobility [24]. The tail states and deep states can be defined as localized states. And the other states are referred as extended states. In these states, the carriers are free to move which are not spatially described. The mobility of carriers in extended states is much higher than that of carriers in localized trap states, because the conduction takes place by a series of trap and release events in localized states. Thus, the mobility is lower than that of the carriers in extended states [25]. The mobility edge concept is frequently used in a-Si due to that the mobility difference in localized states and extended states. The defined cutoff line between the tail states and extended states is called the mobility edge. The mobility inside of the gap depends on temperature and time. The inherent thermal activation process causes temperature dependent of its, and also it is time dependent because of the trap-release time distribution in the band tail and deep states [24].

2.2. Transistor Basics

Actually, a transistor can be defined as a three terminal device in which the current between two terminals is controlled by the voltage (or current) bias applied at the third terminal. There are mainly two type transistors: bipolar junction transistors (BJTs) and field effect transistors (FETs). The operate of a BJT is due to the injection and collection of minority carriers from the third terminal which is called

the base. In these devices, electrons and holes have the important roles; hence, such devices are described as bipolar. Differently, a FET is the majority carrier device, so it can be defined as the unipolar transistor. In addition, the current between two terminals in the FET is controlled by the voltage bias applied from the third terminal which is called the gate.

FETs have various types that depend on how the width of depletion region is modulated. The gate bias controls depletion width of a reverse p-n junction, so this type of transistor is called the junction FET (JFET). On the other hand, both the metal semiconductor FET (MESFET) and the metal insulator FET (MISFET) are a transistor where the gate controls the depletion width of a Schottky junction. However, a MISFET has an additional insulator layer between the metal and semiconductor layers in order to reduce the gate leakage. So, the metal oxide semiconductor FET (MOSFET) is a MISFET that has an oxide layer as the insulator.

In general, transistors are principally used for two processes: switching and amplification. The switching operation can be fundamentally explained as moving a transistor between its on (current passing) and off (current blocked) states. The amplification is an operation that is achieved by applying a small AC signal to the third terminal to generate a larger signal between the other two terminals.

2.2.1 Operation Principles of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

In today's digital and analog electronics industry, the MOSFETs are one of the most often used types of transistors. In a MOSFET device, an electric field is created within the MOS structure in order to control the conductivity of the semiconductor channel between the so called source and drain contacts. The metal contact of the MOS structure is known as the gate terminal of the device.

Basically, n-channel MOSFETs and p-channel MOSFETs are two MOSFETs types. For n-channel MOSFETs, the electrons are utilized as the current carriers, but in other type, the holes are utilized for the current conduction.

Figure 2.3 (a) illustrates the typical n-channel enhancement mode MOSFET structure. In device structure, the n^+, namely highly n-type doped, regions are referred as the source and drain terminals. The thin oxide layer is used to isolate the

semiconductor channel region from the gate metal, so the leakage current from the gate is reduced. To apply voltage bias from the gate terminal and to get electrical contact to the source and drain regions are used the top metal layers.

As shown in Figure 2.3 (b), the FET structure has the formation of two back-to-back p-n diodes, hence there is no current flow between the source and drain regions without an external gate bias. This event can also be understood from the energy-band diagram of the device structure that is demonstrated in Figure 2.3 (c). The potential barrier formed by the p-Si substrate blocks the electrons which is the flow of the majority carriers. If a positive voltage bias is applied from the gate terminal, the holes inside the substrate are repulsed from the oxide - p-Si interface, and so a depletion region is formed that there are no mobile charges in this region. When the gate bias is increased enough, the electrons are taken to this interface to form a conductive channel region which can be named as inversion layer between the source and drain layers. This phenomenon also can be commented as lowering the potential barrier between the source and drain terminals. To decrease the potential barrier and also to form a semiconductor channel region requires a minimum voltage value which is called threshold voltage, V_T.

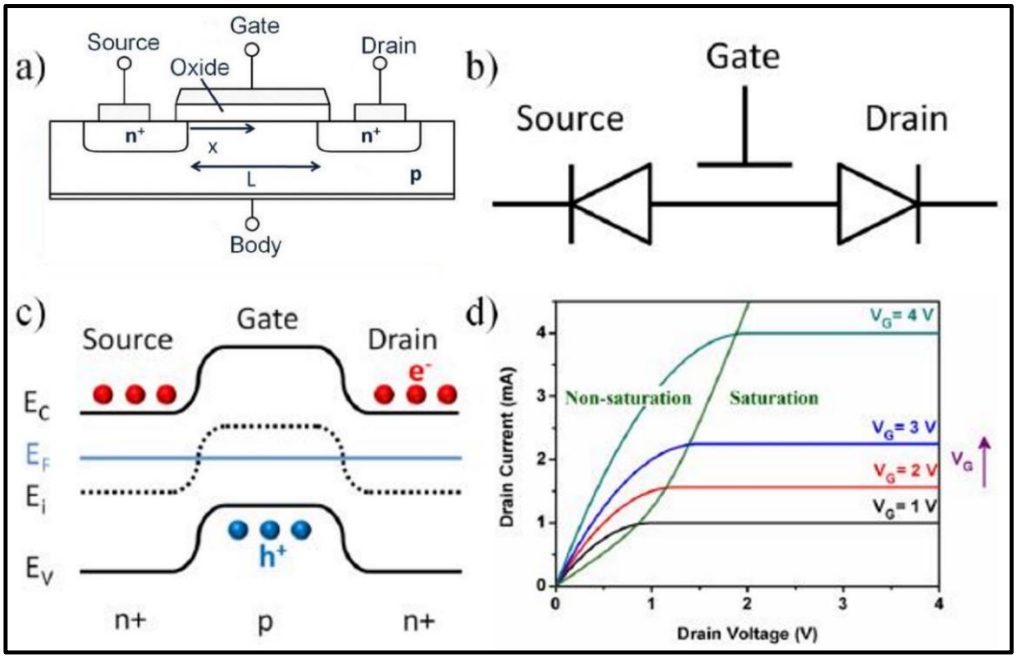

Figure 2.3: The n-channel MOSFET on enhancement mode: (a) cross sectional view of device structure, (b) equivalent circuit in off state, (c) energy-band diagram without voltage bias, (d) typical I_D-V_G characteristic with increasing gate voltage (the green line separates the saturation and non-saturation regions).

Differently from the channel formation of n-type devices, the applying of negative gate bias creates the channel formation in p-type MOSFETs where the electrons are repulsed and the holes are attracted by the negative bias to form a conductive channel. On the other hand, according as the formation of the channel at zero gate bias, MOSFETs shows the behavior of two operation modes. If there is no channel region formation, so described as no current flow from source to drain, at zero gate voltage, this concept is named as enhancement mode of device which is in the off state in normal. Conversely, if a MOSFET has a channel layer, so there is a current flow from source to drain, at zero gate voltage, this event is called depletion mode of device which is in the on state normally. In general, the enhancement mode devices are more chosen to decrease the power consumption at idle state.

2.2.2. Current-Voltage Relations of MOSFETs

There are basically three states of the operation modes of MOSFETs: off, non-saturation and saturation. If the applied gate bias lower than the threshold voltage ($V_G < V_T$), there is no current flow between the source and drain layers and so, the device operates in the off state, as shown in Figure 2.4 (a). For the next, the gate voltage bias equal or larger than the threshold voltage ($V_G \geq V_T$) creates the channel layer formation for a small drain to source bias voltage, V_D that as it is demonstrated in Figure 2.4 (b) and so, the MOSFET operates in the non-saturation mode with a drain to source current, I_D which is given by,

$$I_D = K_n \left[2 \left(V_G - V_T\right) V_D - V_D^2\right] \tag{2.1}$$

where K_n is referred as the conduction parameter and that depends on and is given by as follows,

$$K_n = \frac{W}{L} \frac{C_{ox}\, \mu_n}{2} \tag{2.2}$$

where, respectively, W is the channel width, L is the channel length, C_{ox} is the capacitance of the gate oxide and μ_n is the mobility of electrons in the channel. In here, the W/L ratio is the main and important parameter which allows to simply

design transistors with different drain currents on the same substrate. However, the other parameters are related to the material properties and to change them requires much more effort and cost. When the V_D is applied increasingly, the channel charge density close to the drain region reduces. If the V_D arrives to the saturation drain bias, $V_{D(Sat)}$, this charge density will be zero and so, the device behaves to the saturation mode. The $V_{D(Sat)}$ is described as follows,

$$V_{D(Sat)} = V_G - V_T \tag{2.3}$$

In addition, when the transistor is at the saturation mode, I_D is given by,

$$I_D = K_n (V_G - V_T)^2 \tag{2.4}$$

While the V_D is becoming larger than the $V_{D(Sat)}$, the case which the channel carrier density becomes the zero value and shifts towards to the source region. There is a decline in $V_{D(Sat)}$ voltage between this point and the source. The area between this point and the drain layer is depleted from the mobile carriers and the electrons injected from the edge of the channel region are gathered by the drain with the support of the electric field towards the drain. Figure 2.4 (d) illustrates this operation and also the schematic shape of the channel layer in the MOSFETs.

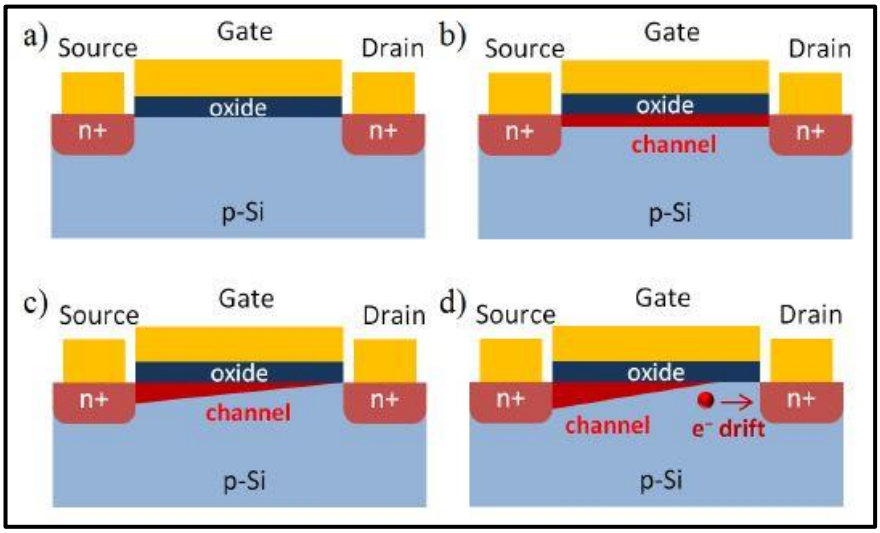

Figure 2.4: Cross sectional view of the n-channel enhancement mode MOSFET for the modes of operation: (a) off state, (b) non-saturation state, (c) passing of the states from non-saturation to saturation, (d) saturation state.

2.3. Thin-Film Transistors (TFTs)

Basically, the TFT is a field effect transistor in spite of the not indirect in its name, so it has three terminals: a source, drain and gate. On the other hand, the structure and operation principles of TFTs are similar to the MOSFET which is the most crucial electronic device component in modern integrated circuits (ICs) of today's. At the same time, the history of TFT and MOSFET development are similar (Figure 2.5) [22]. As seen from the Figure 2.5, the MISFET concept was born in 1925 [26], and the early popular TFTs have consisted of the compound semiconductors such as CdS and CdSe [27, 28]. In addition, the TFT, like the MOSFET, has thin channel, oxide or other insulators/dielectrics and metal contact layers deposited over the nonconductive and supporting substrate. Different from the MOSFETs in which the channel layer is formed inside the substrate, TFTs include a semiconductor film deposited as a channel layer and the substrate in its structure is used for the physical support. The preferred substrates in TFTs are generally the glass substrates that are cheap and transparent. Furthermore, the plastic substrates like PEN and PET are used for flexible TFT applications.

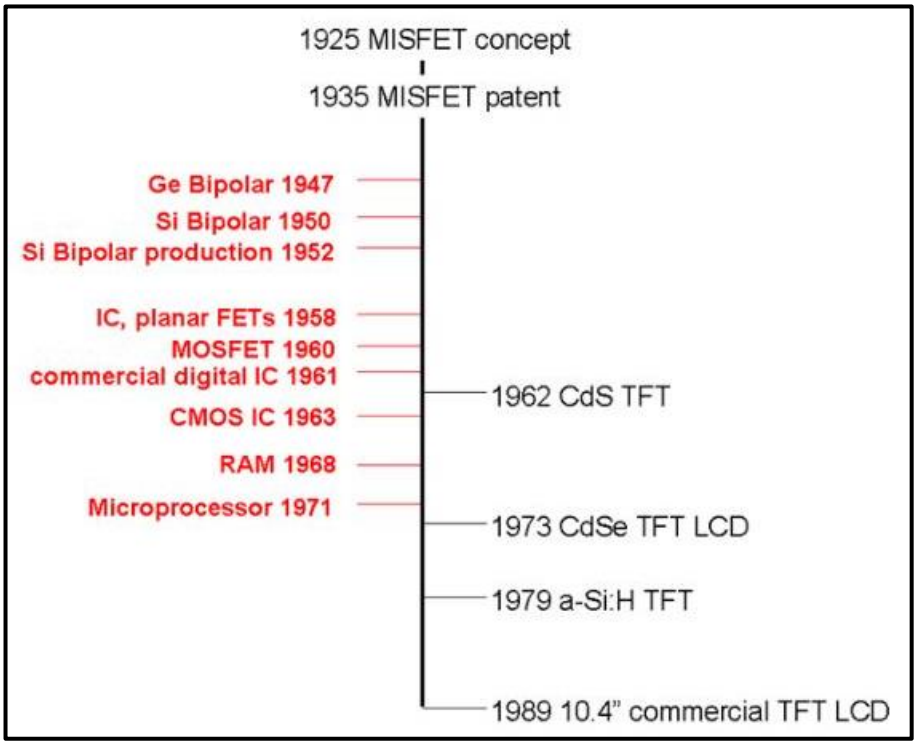

Figure 2.5: The development histories of TFTs and ICs.

For the n-channel enhancement (accumulation) mode TFT, the channel layer is an n-type semiconductor material with low conductivity and the contact metals, i.e. source and drain layers, have ohmic contacts directly to the channel material without highly n-doped regions.

The TFT device operation is typically like that of MOSFET, but this time rather than forming an inversion layer, an accumulation layer forms the channel of the device. And then, the same of stated current-voltage relations for MOSFETs also applies to TFTs. In the case of a n-type TFT, when a positive gate bias is applied, the electrons are attracted to the semiconducting layer from the source and drain terminals and then a conducting channel is created between the two contacts, so the channel has now high conductivity. However, an applied negative gate bias repels the electrons from the channel and decreases its conductivity.

2.3.1. Device Structures

First of all, configuration of device must then be such that an insulating gate dielectric material must be located between the gate metal and the semiconductor channel layer. An applied voltage to the gate metal layer according to the channel should cause an electric field penetrating the channel semiconductor which must end up with a modulation of the carrier concentration and therefore also the current which can flow between the source and drain metal contacts, that are applied to the semiconductor channel directly. It can be said that it is possible to design two general device geometries due to the fact that the semiconducting channel material (in this thesis, intrinsic a-Si:H) is very thin (typically less than 100 nm). Maybe the most clear (and the most like field effect devices on bulk semiconductors) is that the source, drain and gate layers are all on the same side of the channel, and this configuration is named as the “coplanar”. On the other hand, it is also feasible to place the gate on the opposite side of the channel layer to the source and drain, and this structure is called the “staggered”. Moreover, it is feasible to place the gate layer at the top or at the bottom of the stack of thin film materials, and for this reason that these are named as the “top-gate” and “bottom-gate” structures, respectively. Consequently, the four possible basic device configurations which are also the most common structures form due to the above-mentioned explanations: top-gate

coplanar, top-gate staggered, bottom-gate coplanar, and bottom-gate staggered (Figure 2.6) [29, 30].

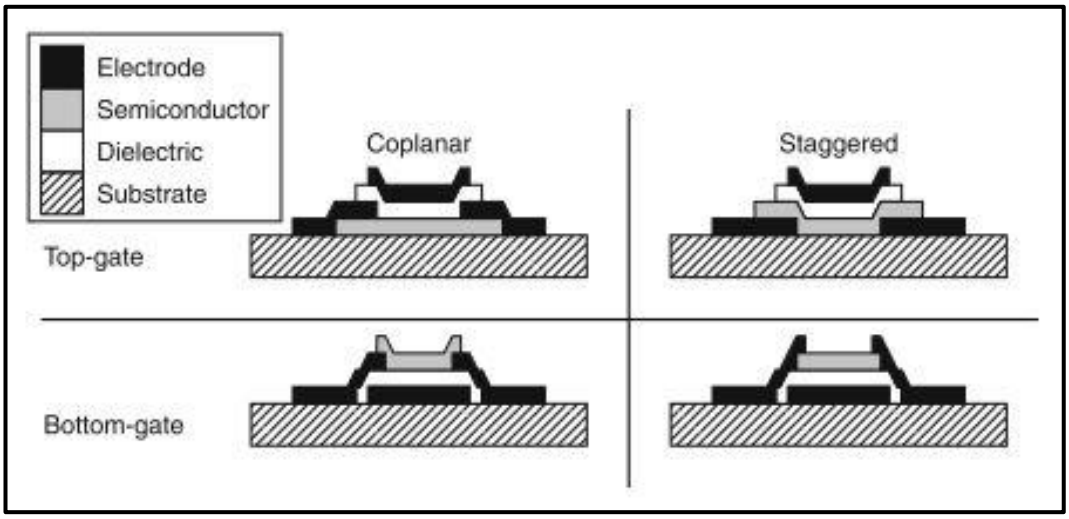

Figure 2.6: The four basic and common TFT device architectures: top-gate coplanar, top-gate staggered, bottom-gate coplanar, and bottom-gate staggered.

The selection of a particular configuration is typically determined by the different steps taken for the TFT fabrication. For instance, in the top-gate coplanar structure, the deposition of the semiconductor channel layer is first made, however the deposition of the insulator or dielectric layer is first made in the bottom-gate structure. The staggered devices, especially bottom-gate concept, have been used for silicon based TFTs and for active-matrix liquid crystal displays because of easy fabrication processing and reliable device performance [31]. In this case, the gate electrode shields light sensitive a-Si from back light emission in AMLCDs. On the other hand, the coplanar structures, particularly top-gate device structure, are more applicable for polycrystalline silicon devices because this configuration allows deposition of thermo sensitive components after high processing temperature of the semiconductor [19, 32]. In addition, the coplanar top-gated structure has another advantage that is encapsulation, providing mechanical and chemical protection of the semiconductor layer from environmental influences that can adversely influence the performance of device [33]. Moreover, for TFT fabrication, top-gate configurations provide a pathway in as little as two steps and with low photosensitivity from upper OLED emissions [34, 35]. For hydrogenated amorphous silicon TFTs, the coplanar configuration is difficult to realize. The a-Si:H TFT devices utilize the ion

implantation method in order to form an ohmic contact to the semiconductor channel. Throughout the ion implantation process, the channel must be protected to avoid the implantation damage. In comparison with the staggered configuration, the coplanar structure has risen the parasitic resistance because of a smaller effective contact area. In the light of this information, the staggered configuration is popular in the a-Si:H TFTs, whereas the coplanar structure is usually used in the poly-Si TFTs.

The double-gated and vertical configurations are among the TFT types different from these basic TFT structures described above, as shown in Figure 2.7 [36]. TFTs with double-gated configuration supply an advanced static performance by controlling a large area of the semiconductor channel, especially in the vertical direction [37, 38]. Moreover, demand for minimal device footprints and channel lengths has caused vertically aligned TFTs (VTFTs) and in this case, the semiconductor channel is defined by thickness of certain layers [39–42].

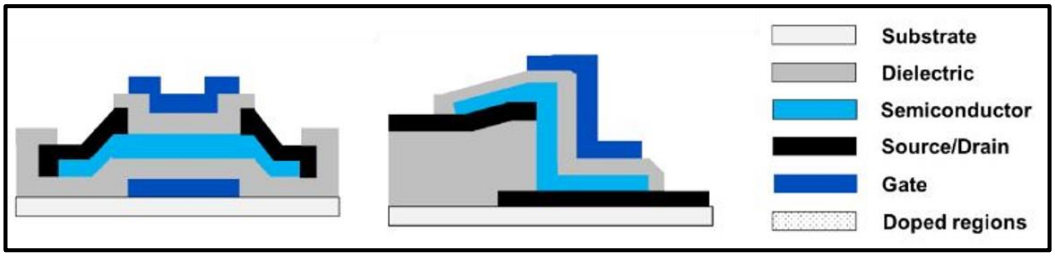

Figure 2.7: The different TFT types: double-gated, vertical.

In this thesis, the fabricated TFT devices are of staggered, not coplanar, top-gate and bottom-gate configurations and these structures and details on its are given in Chapter 4.1.

2.3.2. Thin Film Transistor Materials

The electrical performance of the TFT devices is directly influenced by the constituent materials such as semiconductors and dielectrics. In addition, the different TFT structures mentioned in the previous section can exhibit quite dissimilar device characteristics when using the exact same materials, and it is of great interest. So, semiconductor, dielectric, electrode, and substrate materials for TFTs are introduced below:

2.3.2.1. Semiconductors

The operating of TFTs are based on the field effect on charge carriers in semiconductor materials. This means that the semiconductor material is responsible for the level of device performance, and so that is an integral component of the TFT devices.

Unlike metals, semiconductor materials have temperature related electrical conductivity. For instance, intrinsic, so undoped, semiconductors typically exhibit increasing electrical conductivity in response to rising temperature as the charge carrier's concentration increases. However, metals experience increased resistivity to enhanced temperature due to increased electron/phonon interactions in metal lattice. Semiconductor materials have higher electrical resistance than metals, however lesser resistivity than insulators [43]. This difference between these materials is explained by the electrons inside material in terms of density of states. DOS defines the number of available states for electrons to occupy per interval in each energy level. For large DOS, there are a large number of available states for electrons to occupy. On the contrary, a DOS of zero means that no electrons can occupy a given energy level. In DOS, band gap determines electrical conductivity of solid materials. A large band gap results in higher electrical resistivity in organic (plastic) or ceramic insulators. Very small or no band gap, so overlap of conduction and valance bands, results in the high conductivity of metals. Semiconductors have smaller band gap than insulators, however larger than metals, as shown in Figure 2.8. Figure 2.8 indicates the relation between band gap and conductivity, where the Fermi level defines the energy at 0 K below which all of the available states are occupied and above which no states are filled. For the temperature at 0 K above, electrons can be excited into states above the Fermi level as showed by the grey shading in Figure 2.8. There are three types of semiconductors: one intrinsic and two extrinsic including p-type and n-type, as presented in Figure 2.8. Changing the concentration of mobile charge carriers at thermal equilibrium, extrinsic semiconductors are doped by the addition of impurity species. Doped semiconductors are categorized as p-type and n-type with respect to the concentration of dominant charge carriers. Dopant species can be electron donors or acceptors. Donor dopants have more valance electrons than the species they replace, providing extra electrons to the conduction band of the

material and enhancement the material's negative charge carrier concentration. Semiconductor materials with so great concentration of negative charge carriers are called n-type. Acceptor dopants have lesser valance electrons than the species they replace, accepting electrons from the valance band of the material and increasing the material's positive charge carrier concentration, this case makes it p-type. Unlike the extrinsic semiconductor materials, the concentration of charge carriers in intrinsic semiconductors is a property of the material itself, not a result of doping. For instance, holes in an intrinsic material's valance band can arise from thermally generated electron excitation to the conduction band, not from electron loss to an acceptor dopant. In the n-type semiconductors, the Fermi level is closer to the conduction band than the valance band than it is for intrinsic semiconductors, but the Fermi level in the p-type semiconductors is closer to the valance band than the conduction band, and these relations are shown in Figure 2.8.

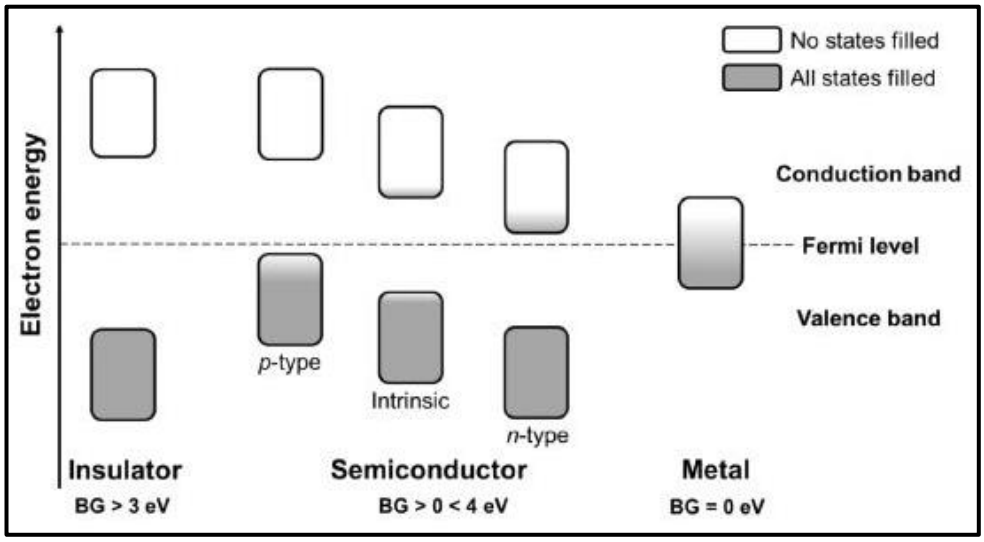

Figure 2.8: Bandgap of different materials based on occupation of energy states by electrons.

There are three main groups of TFT semiconductor materials: silicon types, metal oxides, and organic species. The high mobility and flexible substrates are two important functionalities for TFTs. All TFT applications take advantage of a high on current that is proportional to carrier mobility. Simple switches and on-pixel circuits such as preamplifiers can be applicable with n-channel TFTs. Monolithic integration with peripheral circuits and reduction of power consumption require also p-type TFTs. OLEDs also use p-channel TFT current sources due to their particular contact

configuration. The grain size of silicon films takes on predominant importance because of the need for high mobility, regardless of the substrate material on which the silicon is deposited. As a result, the correlation between mobility/grain size and process temperature dominates the research on channel materials for silicon TFTs. By applying a maximum process temperature of ~600°C, glass substrates have forced the invention of low temperature processes for device fabrication and for the crystallization of precursor layers. Steel substrates allow the adoption of many processes used by the integrated circuit industry, this is achieved by tolerating temperatures of close to 1000°C. On the contrary, the low temperature stability of organic polymer substrates, such as plastic, needs a broad revision of TFT materials, device configuration, and processes. a-Si TFTs can be brought to plastic by careful adaptation of the set to 250–350°C processes to the temperatures of 150°C or less tolerated by plastics. With their top gate structure, SiO_2 dielectric, and decreased tolerance to series resistances, TFTs with high mobility made from directly deposited nc-Si or from laser crystallized μc-Si pose much greater challenges to fabrication on plastic. Making the auxiliary materials that includes a stable gate dielectric and highly conducting contacts at temperatures of ~100°C can turn out to be more demanding on the fabrication of silicon TFT CMOS on plastic substrates than the preparation of the channel material itself. Figure 2.9 demonstrates the modifications of silicon available for TFTs, as well as approximate regimes of carrier mobility and types of device, in this case that the grain size is used as the operation parameter [44].

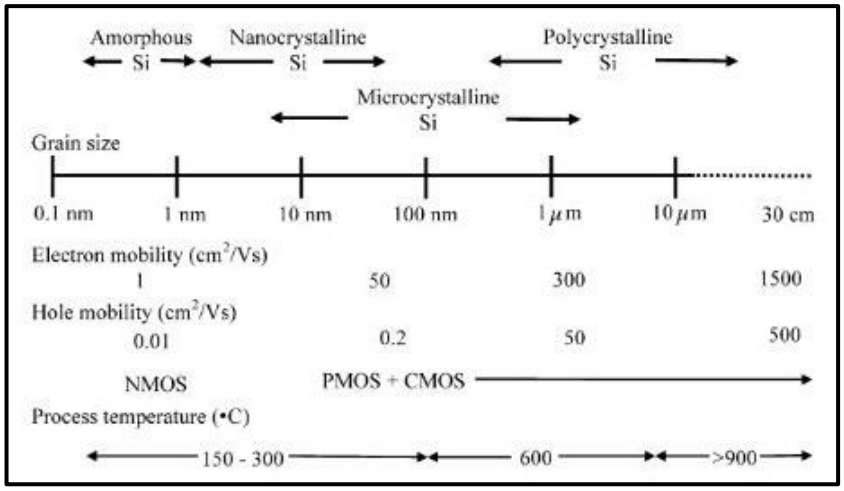

Figure 2.9: Modifications of silicon films available for TFT fabrication, with associated carrier mobilities, FET capability, and process temperatures.

In addition, the three grades of thin film silicon that are available for the fabrication of TFT backplanes are listed in Table 2.1 [45]. It is possible that amorphous silicon backplanes are made at the standard process temperature of 250–350°C on stell [46, 47] and at ~100–150°C on plastic [48–52] foil substrates. Nanocrystalline silicon TFTs [53–57] can be made at the same low temperatures as a-Si, and also with p or n channels. Therefore, they are capable of CMOS, however their device and process technology are immature [56]. Micro or poly crystalline silicon supplies CMOS with the highest mobilities, however needs high temperature processing [58, 59]. For steel substrates, furnace processing can be accepted. Laser crystallization for steel [60, 61] and plastic [62] substrates has been studied.

Table 2.1: Properties of silicon materials for TFTs.

Attribute	**a-Si:H**	**nc-Si:H**	**μc-Si**
Standard deposition T [°C]	250	250	150 (precursor)
Highest T process/material [°C]	350 SiN_x	280 n^+, p^+	Laser μc-Si
Lowest reported process T [°C]	110	150	Laser
Electron mobility [$cm^2 V^{-1} s^{-1}$]	0.5 – 1	40	300
Hole μ [$cm^2 V^{-1} s^{-1}$]	~ 0.01	0.2	50
Conductivity [$S\ cm^{-1}$]	10^{-11}	10^{-7} – 10^{-2}	10^{-6}
Growth rate [$nm\ s^{-1}$]	0.1 – 1	0.1	0.1 – 1
Gate and source/drain geometry	Top and bottom Staggered	Top Coplanar or staggered	Top Coplanar
Gate insulator	SiN_x	SiO_2	SiO_2

PECVD deposited a-Si:H films at temperatures of 250–350°C are a well-characterized baseline process and provide reproducible material. PECVD for the deposition of device-grade silicon at 150°C offers an advantage that requires only an extension instead of a new deposition method. This advantage is showed with the measurements of field effect mobilities in a-Si:H ($\mu_n \cong 0.5\ cm^2V^{-1}s^{-1}$) and in nc-Si:H ($\mu_n \cong 40\ cm^2V^{-1}s^{-1}$ and $\mu_p \cong 0.2\ cm^2V^{-1}s^{-1}$) deposited at 150°C [57]. Low temperature processing needs the re-optimization of all high temperature steps. The quality of PEVCD deposited a-Si:H and SiN_x films is deteriorated with decreasing temperature of deposition. The source gases are diluted with hydrogen in order to overcome this problem, so this improvement ensures that the electronic properties of

a-Si:H and SiN_x layers are comparable to those of a-Si:H/SiN_x grown at the optimum temperature of 250–350°C. The most critical re-optimization is that of the highest temperature process and material, where a device process is brought from high to low temperature. It is known that SiN_x is used as the gate dielectric in the a-Si:H TFTs. In terms of a good device quality, SiN_x gate dielectric deposited at the standard temperatures of 300–350°C usually is slightly nitrogen rich. When the refractive index of the SiN_x layer is in the range of 1.85–1.90, the threshold voltage in TFTs is the lowest. The refraction index is related to the stoichiometry of the film, being larger for films with silicon rich. S. Wagner et al. have studied that their optimized 150°C film has a growth rate of 1.5 Å s^{-1}, refraction index n=1.80 at the wavelength of 632.8 nm, dielectric constant ε=7.46, dielectric breakdown field > 3.4 MV cm^{-1}, Si/N ratio of 0.67, and H content of ~$2x10^{22}$ cm^{-3} [53]. On the other hand, the fabrication of nc-Si:H TFTs requires considerably more research than that of 150°C a-Si:H TFTs. There are two consequences of the structural evolution of nc-Si from amorphous close to the substrate to increasingly granular as the film grows thick. The first one is an enhancement in the carrier mobilities in the top layer of the film. The electron field effect mobility increases from that in a-Si:H to ~40 $cm^2V^{-1}s^{-1}$ and the hole mobility to ~0.2 $cm^2V^{-1}s^{-1}$ in completely connected nc-Si layers. It is possible that the maximum mobility values rise up with progress in device fabrication. The enhancement in mobility with thickness of film makes think the change in the dominating mechanism, from trapping and re-emission out of bandgap states to emission over electrostatic barriers at grain boundaries. nc-Si device structure gives information about why top gate nc-Si TFTs exhibit much higher field effect mobilities than bottom gate devices. For the evolution of a-Si:H → nc-Si, a second consequence is the electrical activation in nc-Si of impurities, so unwanted, that are inactive in a-Si:H. From the researches about solar cell, it is already known that the electrical conductivity of nominally undoped nc-Si can be too high. When the conductivity of intrinsic crystalline Si is ~10^{-5} S cm^{-1}, that of not intentionally doped nc-Si can reach 10^{-2} S cm^{-1}, and can be brought to values as low as 10^{-7} S cm^{-1}. The care must be taken to keep the thickness-averaged electrical conductivity of the channel layer low, and still grow a top layer with high field effect mobilities, due to that the off current of TFTs is set by the conductance of the channel layer. This concept provides low off current and high on current and can be obtained by careful adjustment of nc-Si deposition conditions and thickness of layer, which can be as

low as 50 nm or as high as 300 nm [63]. Moreover, the furnace crystallization of a-Si precursor films to microcrystalline silicon films is an established technology for TFTs, and also laser crystallization on glass substrates has entered industrial production. If the devices of poly-Si films are fabricated on steel foil substrates, it is a simple extension of the crystallization on glass however with greater process latitude. Laser crystallization of a-Si on plastic substrates and then fabrication of TFTs are one of the experimentally most challenging aspects in TFT research. μc-Si TFTs also including that μc-Si TFTs fabricated on steel foil require a separate discussion [63].

The oxides of post transition metal elements are the second key group of semiconductor materials for TFT channels. There are several materials used in amorphous oxide semiconductors (AOSs) [64, 65], but amorphous InGaZnO is a popular channel material. a-InGaZnO TFTs have an importance in other electronic devices due to their enhanced performance in terms of mobility, stability, spatial uniformity and transparency to visible light. A few years ago, zinc oxide (ZnO) has developed as a substitute material for TFTs under large area operations. ZnO is a wide bandgap semiconductor with ~3.3–3.4 eV of II-VI semiconductor group, which has high electron mobility, efficient photon emission and can be easily n-doped. Moreover, GaN based TFTs have drawn attention in research area in fields of high speed, high power and high processing temperature because of better transport properties of 2D electron gas channel [66]. To place high quality GaN thin films using low cost substrate under low temperature, is one of the research areas in this field. Furthermore, low electrical stability of ZnO TFTs also affects the commercialization of these devices [67]. Consequently, n-channel GaN TFTs with structures of top-gate and bottom-gate are fabricated, which have good electrical performance and low processing temperature [68, 69]. These GaN TFTs play an important role in the next generation of flat panel displays. Lastly, organic materials such as pentacene or thiophene derivatives are the third main group of semiconductor materials for TFT channels. Organic thin film transistors (OTFTs) have attracted attention due to future applications of devices including flexible displays, smart cards and ID tags [70–72]. The performance of devices has been greatly improved in last few years. Pentacene TFTs with Al_2O_3 gate dielectric on Si substrate have been reported to be 5 cm^2/Vs of the field effect mobility [73]. Organic semiconductors are suitable for fabricated on various plastic substrates at low temperatures, therefore can

be placed on the substrates at such temperatures [74, 75]. OTFTs are parallel to inorganic ones in terms of basic function and design. The on/off current ratio increases the switching performance of OTFTs up to 10^6 [17, 18]. As compared to the bottom-gate devices, top-gate devices have been studied to give better results due to reduced contact resistance, but there are several challenges in this field which include stability of OTFTs in the air, alignment organic molecules and large driving voltage [76]. Despite the fact that there are numerous studies on OTFT characteristics and structure, however the conclusions are complex and diverse in nature [76–79]. This case arises from the issue of the difference between the structure and the process effects, but the dependence of OTFT characteristics on the structure is examined using 2D simulation. It explains that OTFT with staggered structure has better electrical performance than OTFT with coplanar design [80]. In view of Schottky barrier contact, OTFT with staggered design has higher current flow, lower contact resistance and higher field effect mobility than coplanar one.

a-Si:H is the semiconductor selected for TFT devices fabricated during this thesis study. a-Si:H material is prepared and deposited by PECVD technique as a thin film.

2.3.2.2. Dielectrics

In a-Si:H TFTs, dielectric thin films are used in three main purposes: gate dielectric, channel passivation, and completed transistor passivation. Also, before the TFT fabrication, a dielectric film is commonly used as the substrate passivation or diffusion barrier layer. All of the TFT characteristics are directly affected by the properties of the dielectric material and its deposition process. For instance, if PECVD deposited SiN_x is used as the gate dielectric material, it affects the channel current path; if it is used as the channel passivation layer, it may influence the leakage current and photoleakage current. The fixed charge at the a-Si:H/SiN_x interface can bend the band at the gate dielectric/a-Si:H interface, which affects many of the main transistor characteristics. When the a-Si:H channel layer of a TFT is very thin, its interface properties which are highly based on the following dielectric deposition condition, may influence the channel operation region. Moreover, a stress mismatch between a-Si:H channel and the dielectric layers, which

is commonly observed, may affect the characteristics of TFT. On the other hand, the a-Si:H TFT performance is extremely depended on its structure. For instance, the inverted staggered a-Si:H TFT has different transistor characteristics from the staggered a-Si:H TFT at the same deposition conditions due to that their gate dielectric interfaces are different. Moreover, it is usually known that the bottom-gate (inverted, staggered) device has better characteristics than the top-gate (normal or staggered) device in spite of that both TFTs were made from the same a-Si:H and SiN_x deposition conditions. Figure 2.10 demonstrates the transfer characteristics of top-gate and bottom-gate devices, where all films were deposited at the same process conditions apart from the sequence [81]. The sequence of a-Si:H/SiN_x deposition affects many physical and chemical properties at and near the interface region. When compared with the staggered device, the inverted staggered device has a higher μ_{eff}, lower V_{th}, lower S, higher I_{on}, and lower ΔV_{th}. In addition to all these, for the same TFT structure, different back channel dielectric passivation layers can result in different transistor performance.

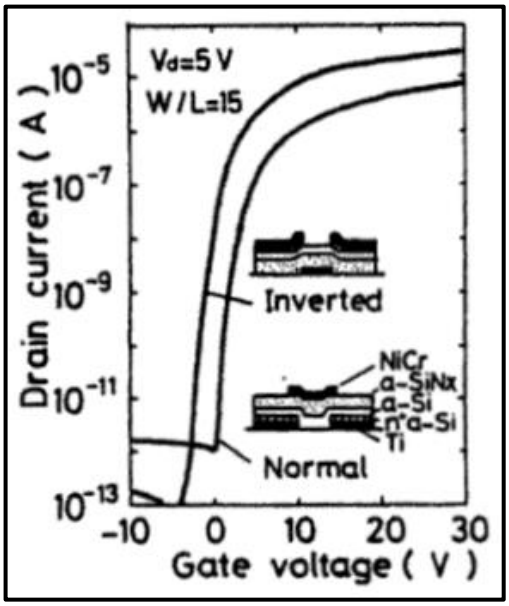

Figure 2.10: The transfer characteristics of top-gate and bottom-gate a-Si:H TFTs at the same film deposition conditions.

Because of that the gate dielectric material plays an important role in the a-Si:H TFTs, a very large amount of research and development works have been performed to study about the deposition process and its effect on the transistor characteristics. The most commonly investigated physical properties of the dielectric

film contain dielectric constant, stress, thermal stability, composition, binding energies, and etc. These dielectric parameters influence the electrical properties of the film, such as charge trapping density, flat band shift, and breakdown voltage, V_{bd}, which further influences on characteristics of TFT, such as field effective mobility, μ_{eff}, threshold voltage, V_{th}, on and off currents, I_{on} and I_{off}, and subthreshold slope, S. The parameters to be investigated for the large area dielectric film deposition include: deposition rate, thickness and composition uniformities, step coverage, throughput, particles, chemical contaminations, pinhole density, and etc. Because of that the low process temperature is the main limitation in the a-Si:H TFT fabrication, nearly all common low temperature dielectric materials have been used to fabricate of TFTs in order to investigate their effects on transistor characteristics. For instance, different types of gate dielectric films were growth by LPCVD, atmospheric pressure CVD, APCVD, PECVD, remote plasma CVD, photo CVD, catalytic CVD, thermal evaporation, sputtering, liquid phase deposition, anodization of a metal, and spin coating techniques. Both inorganic and organic dielectric materials such as silicon nitride, silicon oxide, silicon oxynitride, tantalum oxide, aluminum oxide, and benzocyclobutene, BCB were used to test. Moreover, the dual-layer dielectric structure, i.e., a separate interface layer from the bulk gate dielectric film as shown in Figure 2.11 (a), is commonly used in the large area TFT array fabrication to achieve the optimized transistor characteristics. The bulk dielectric material can be a metal oxide or a silicon nitride film, however the interface layer is commonly a silicon nitride film. Figure 2.11 (b) demonstrates that the field effect mobility, μ_{eff} of the a-Si:H TFT with two different SiN_x layers is higher than that with one SiN_x gate dielectric layer [82]. The addition of a proper interface layer can decrease the interface stress and density of states. Also, the dual-layer structure improved the production yield due to the better step coverage and reduction of chemical attack in the subsequent etching or cleaning step.

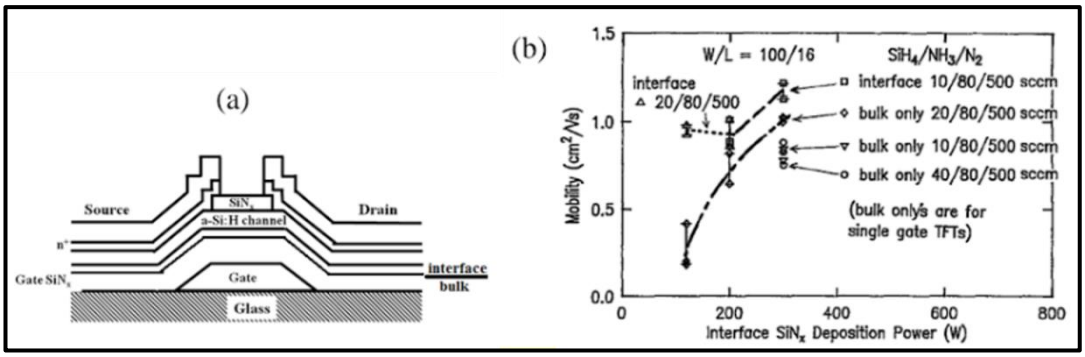

Figure 2.11: (a) TFT with a dual-layer gate dielectric, (b) interface SiN_x effect on μ_{eff}.

Figure 2.12 shows the transfer characteristics in the top-gate, bottom-gate, and dual-gate mode operations of a dual-gate PDPP-TNT TFT. The inset in the Figure 2.12, demonstrates that the current density from a dual-gate device is larger than the sum of current densities of both top-gate and bottom-gate devices [83]. When compared with the top-gate and bottom-gate, dual-gate mode operation gives the lowest V_{th} and improvements in subthreshold swing, S.S. and on/off current ratio.

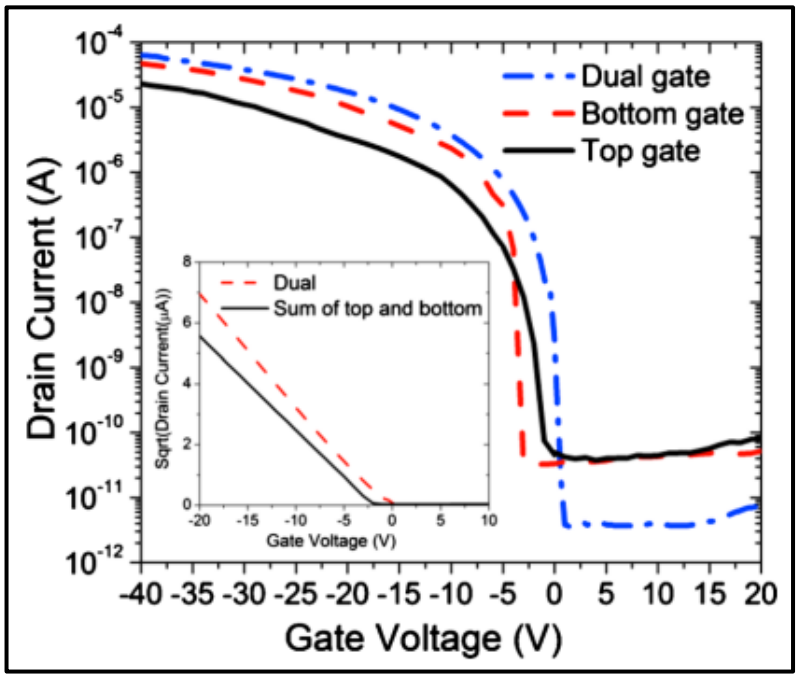

Figure 2.12: The transfer characteristics in the top-gate, bottom-gate, and dual-gate modes of a dual-gate PDPP-TNT TFT.

For practical applications, the dielectric film deposition requires to be coherent with that of the a-Si:H channel layer in areas such as low temperature, simple

operation, minimum interface damages, high throughput, and large area capability. So, PECVD is the ideal technique for this application for various reasons: the a-Si:H layer is commonly deposited by PECVD, the a-Si:H/dielectric layers can be deposited in one-pump-down to reserve clean interfaces, the dielectric material properties can be easily adapted to match those of a specific a-Si:H layer for the optimized characteristics of TFT, and the interface properties can be optimized by inserting a plasma step between two deposition steps. PECVD deposited silicon oxide, SiO_x and silicon nitride, SiN_x have been used as gate dielectrics in the fabrication of a-Si:H TFTs. The TFT with the SiN_x gate dielectric has a lower S, and a smaller V_{th} than those of the TFT with the SiO_x gate dielectric [84]. So, PECVD SiN_x has been proved superior to PECVD SiO_x as the gate dielectric of a-Si:H TFT. Consequently, it is widely known that PECVD deposited SiN_x is most preferred than other dielectrics as the gate dielectric layer of an a-Si:H TFT. The PECVD SiN_x dielectric film should be slightly nitrogen-rich, and include a large amount of hydrogen such as 20% or higher, for the a-Si:H TFT gate dielectric application. This case is different from the traditional VLSI dielectric requirements that the film should be near stoichiometric and includes a low hydrogen concentration. The relations between characteristics of TFT and SiN_x dielectric film properties are very complicated or detailed. The TFT performance is affected by the physical and chemical properties of the film, such as the Si/N ratio, the NH/SiH ratio, stress, and the hydrogen content, which are all critical.

For this thesis study, a dual-layered gate dielectric structure is used in the fabrication of a-Si:H TFTs, which includes PECVD deposited SiN_x and ALD growth Al_2O_3 films as gate dielectric layers. Also, SiN_x film is used for the passivation layer.

2.3.2.3. Contacts

In TFTs, a wide variety of conductive materials are suitable for gate, drain, and source terminal contact electrodes. For instance, a research on metals demonstrated a variety of gate contact materials including Cr, Ti, Cu, and Pt had only a slight effect on electrical performance of IGZO TFTs [85]. Many other metals are used as TFT gate contact materials including Al [86], Mo [87], Au [88], Ni [89], and metal alloys or blends including MoTi [90], TaN [91], AlNd [92]. In addition to metals, oxide

materials such as indium tin and zinc oxides, ITO/IZO [93, 94], aluminium zinc oxide, AZO [95], and indium oxide, In_2O_3 [96] are employable as TFT gate contacts. The conducting a large current in a TFT device does not require the gate electrode and therefore the compatibility with the fabrication process is a limiting factor in determining the choice of gate contact material [36].

Source and drain electrodes in TFTs need high electrical conductivity and limited contact resistance, R_c with the semiconductor material [36]. Metals are a common material used for source and drain electrodes in TFTs because of their high electrical conductivity. Examples include Al [97], Mo [87], Ti [39], Au [98], Cu [99], and Pd [100]. However, it is difficult to create an ohmic contact with the semiconductor material. To perform ohmic contact, materials require good charge injection and lower R_c at the semiconductor/contact interface. Multi-layered contacts are one approach in reducing R_c. This structure includes depositing a layer of adhesion promoting metal at the semiconductor interface under the bulk contact material. For instance, Cr/Au [101], Mo/Al [97], Ni/Au [102], Ti/Au [103]. On the other hand, metals do not generally provide optical transparency and therefore transparent conducting oxides, TCOs such as ITO [104] and IZO [105] can be used for these applications.

The gate, source, and drain electrode layers for this thesis study are sputtered Cr thin film.

2.3.2.4. Substrates

Fabrication of TFTs typically contains deposition of sequential layers onto a certain material that might (e.g. dielectric) or might not (e.g. insulator) affect the operation of device. A substrate is such a material, the choice of which depends on factors containing the intended device application and process conditions. For instance, glass substrate is applicable as transparent, insulating TFT substrate material, however is not flexible [106]. Plastic substrates such as polyethylene naphthalate, PEN [107], polyethylene terephthalate, PET [108], and polyimide, PI [109] are used where both transparency and flexibility are needed. However, process temperature restricts the use of plastic substrates because of that many polymers are not thermally tolerant, having large thermal expansion coefficients, CTE and low

glass transition temperatures, T_g leading to limit flexibility on the rise of temperature. Moreover, such polymers suffer moisture/gas permeation and may not be complete insulators [31]. Another TFT substrate is paper which is cheap and environmentally sound, but not thermally stable or resistant to moisture/gas permeation [102]. Si materials are generally thermally tolerant substrates, while neither flexible nor transparent. Silicon wafer is useful as a substrate for fabrication of reference devices [110].

Table 2.2 shows a chart of compatibility of silicon with the main groups of substrate materials [44]. Due to that steel foil can be processed up to 1000°C, all conceivable silicon TFT fabrication, from a-Si:H to μc-Si, can be applied on it, like on glass. On the other hand, steel substrate is opaque and couples in a large parasitic capacitance. Plastic foils can be transparent and even clear, however may be processed up to only 100 or 200°C. In addition, plastic substrates present many new challenges, which have been recognized only in part.

Table 2.2: The compatibility of directly deposited silicon channels with substrate materials.

Substrate material and T limit	**Plastic**	**Glass**	**Steel**
TFT use	≤ 150 °C	≤ 600 °C	≤ 1000 °C
Preferred for cell switch (n channel)	a-Si:H	a-Si:H	a-Si:H
Preferred for peripheral circuits (n and p channel)	nc-Si:H	μc-Si or nc-Si:H	μc-Si or nc-Si:H

This thesis study relied on glass substrates, which is type of Corning Eagle XG.

2.3.3. Thin Film Transistor Operation and Performance

This section reports TFT key performance indicators, and explains how devices are electrically characterized. In TFT operation, the key direct current (DC) electrical performance parameters are from current-voltage characteristics according to the gradual channel approximation [31, 111]. Plotting of two forms of current-voltage data relations gives information about electrical characteristics of TFTs. First one is a logarithmic plot of I_D over V_G which provides a transfer curve including gate current leakage, I_G plotted over V_G. Second one is a logarithmic plot of I_D over V_D which

gives an output curve. These curves have two key operating regimes which are linear and saturation [36]. The linear regime holds for small values of V_D where $V_D << V_G – V_{th}$. In this case, I_D may be approximated according to the Shichman-Hodges model [112], and which is defined as follows,

$$I_{D,lin} = \frac{W\,\mu\,C_{ox}}{L}\,(V_G - V_{th})\,V_D \tag{2.5}$$

where μ is mobility of free charge carriers, C_{ox} is capacitance, which is generally defined as the ability for storage of electrical charge, of the gate dielectric per unit area, and L is TFT channel length. For larger values of V_D where $V_D \geq V_G – V_{th}$, TFT devices operate in saturation regime with I_D which is given as follows,

$$I_{D,sat} = \frac{W\,\mu\,C_{ox}}{2L}\,(V_G - V_{th})^2 \tag{2.6}$$

As mentioned above, Equations 2.5 and 2.6 consider the channel dimensions L and W. The reason for this is that the physical shape and size of a TFT influence the electrical performance of device, with optimum devices having semiconductor and dielectric thickness that is much smaller than the L, with W around 15 times larger than L [27].

Linear extrapolation of the I_D/V_G transfer curve for linear regime, or $I_D^{1/2}$-V_G curve for saturation regime, gives V_{th} [113]. On/off current ratio, I_{on}/I_{off} is the ratio of maximum to minimum I_D, typically in the saturation regime [111]. Maximum I_D is inherent in the semiconductor material due to the effectiveness of field effect accumulation of charge carriers. Minimum I_D may be based on background instrument noise, or I_G. Large $I_{on}/I_{off} \geq 10^6$ is typically needed for TFT devices as useful I_D switches [114, 115]. On the other hand, $I_{on}/I_{off} \geq 10^6$ is enough for analog circuitry [93]. Turn on voltage, V_{on} is the value of V_G where a conductive channel forms, enabling I_D>zero, because of field effect accumulation of charge carriers. In a transfer curve of the TFT device, V_{on} is evident as the point at which I_D begins to increase, the V_G required to turn the device off [116].

Overlap capacitance, C_{ov} between the source-drain and gate electrodes has an effect on the speed of TFT device operation and which is obtained by first considering a relation of total gate capacitance, C_G [36, 111],

$$C_G = C_{GS} + C_{GD} = C_{ox} W (L + L_{ov+tot}) \quad (2.7)$$

where C_{GS} is the gate-source capacitance, C_{GD} symbolizes gate-grain capacitance, and L_{ov+tot} is total overlap length between the source-drain and gate electrodes [111]. Equation 2.7 provides construction of a plot of C_G over V_G, with C_{ov} found to be the minima of C_G [36].

Transit frequency, f_t gives information about the speed of a TFT device and can be described as follows [111, 117],

$$f_t = \frac{1}{2\pi} \frac{g_m}{C_G} \left(\frac{\mu (V_{GS} - V_{th})}{L (L + L_{ov+tot})} \right)^{-1} \quad (2.8)$$

where g_m is the transconductance in the saturation regime, and which is expressed by the following equation [118],

$$g_m = \left(\frac{dI_D}{dV_G} \right) \Big|_{V_D} \quad (2.9)$$

Note that the transconductance is the ratio of current change to voltage change, in this case referring to the ratio of changes in I_D and V_G, respectively.

Subthreshold swing, S means to the V_G needed to increase I_D by one decade. This helps to understand how efficiently a TFT device can switch between on or off states and is related to the semiconductor/dielectric interface quality [36, 111]. Small S allows low power consumption and high speed of TFT devices, with ideally $S << 1$ [119]. S is the inverse of the TFT transfer curve slope maxima according to following relation [19, 36],

$$S = \left(\frac{d \log_{10}(I_D)}{dV_G} \Big|_{max} \right)^{-1} \quad (2.10)$$

In a TFT device, μ is a measure of efficiency of charge carrier movement. High μ provides high I_D, allowing rapid f_t. Factors limiting μ contain scattering of charge carriers by structural defects including grain boundaries, interfacial roughness, impurities, and lattice vibrations. Several methods follow that apply for

determination of TFT μ as defined by Schroder [120]. Effective mobility, μ_{eff} from drain conductance, g_d with a low V_D, can be explained as following relation,

$$\mu_{eff} = \frac{g_d}{C_{ox}\frac{W}{L}(V_G - V_{on})} \tag{2.11}$$

where g_d is obtained from the following equation [118],

$$g_d = \left(\frac{dI_D}{dV_D}\right)\Big|_{V_G} \tag{2.12}$$

Field effect mobility, μ_{FE} from g_m with low V_D,

$$\mu_{FE} = \frac{L}{W\,C_{ox}\,V_D}\,g_m \tag{2.13}$$

Saturation mobility, μ_{sat} from g_m with a high V_D,

$$\mu_{sat} = \left(\frac{d\sqrt[2]{I_D}}{dV_G}\right)^2 \left(\frac{1}{2}\,C_{ox}\,\frac{W}{L}\right)^{-1} \tag{2.14}$$

In general, literature only gives the peak values for μ_{eff}, μ_{FE}, and μ_{sat}. On the other hand, plotting of these factors as a function of V_G can highlight μ degradation arising from scattering or contact resistance relative to increasing V_G [19].

R_c between the source-drain contact electrodes and semiconductor channel material has a special importance in short channel TFT devices with $L \leq 5$ μm, where high R_c may result in poor f_t and μ_{FE} [121]. R_c is influenced by such things as the semiconductor/contact interface, and interfacial treatments, as well as the source-drain electrode material [122–124]. Analysis of the transfer curves of a set of TFT devices with changing L gives a value for total resistance, R_T, according to the formula below,

$$R_T = R_{ch}\,L + R_c \tag{2.15}$$

where R_{ch} is the channel resistance per unit of channel length [124]. Plotting R_T values at changing V_G provides determination of R_c. Another method is that R_c can

be obtained from the ratio of two transfer curves from the same TFT device, recorded at two different V_D values [125].

In brief, rapid switching between on or off state is desirable for TFT devices. To provide this case needs very small S, V_{th} close to zero, and high μ [31]. Electrical characterization of TFT devices in the form of transfer and output curves not only ensures quantitative device information in the form of the parameters described above, but also gives a qualitative visual indication of TFT device performance.

3. EXPERIMENTAL TECHNIQUES

This chapter provides the experimental details of the works covered in this thesis. The first and second part of the chapter includes the description of the fabrication process and equipment, and the third part provides the electrical characterization of the devices. The experiments are conducted in the cleanroom (class 100 and 1000, FED STD) of Photonic Technologies Group Laboratories (FESLAB) at TUBITAK.

3.1. Thin Film Deposition Process and Equipment

In this study, PECVD, ALD, and sputtering techniques are used for thin film depositions in the fabrication of transistor devices.

3.1.1. Plasma Enhanced Chemical Vapor Deposition (PECVD)

Plasma enhanced chemical vapor deposition (PECVD) is the popular method used today for the deposition of a-Si and amorphous insulator materials used in large area electronics applications. Its relatively low processing temperature and ability to produce uniform growth over large areas has caused widespread acceptance by display and photovoltaics industries.

As the name suggests, the driving force behind PECVD is the plasma. The plasma is created in a gaseous precursor by applying a large electric field. The electric field ionizes the gas molecules creating electrons and ions, and then, due to their smaller mass, the electrons are accelerated to high speeds by the applied electric field. The high speed electrons can then give their large kinetic energy to other gas molecules via collision, and these collisions create more excited electrons and ions, as well as highly reactive neutral species. The colored glowing that is characteristic of the plasma is related to the release of photons during the relaxation of gas molecules and ions from the excited states. While the highly reactive species, also named as radicals, are responsible for the growth on the substrate surface, the excited electrons and ions continue the collision and excitation processes. In order to support the dissociation of the precursor gases and increase the surface mobility of the

radicals on the growing surface, the substrate and the reaction chamber are often heated to moderate temperatures (150–400°C). The properties of PECVD deposited materials depend on the substrate temperature, precursor gas composition and flow rate, chamber pressure and applied electric field [25].

The PECVD systems with radio frequency (RF) at 13.56 MHz are used for the deposition of a-Si and related semiconductor/insulator materials in this thesis. Ultra high vacuum Plasma Enhanced Chemical Vapor Deposition system at TUBITAK MAM ME is shown in Figure 3.1. This system contains two capacitively coupled plasma chambers for the deposition of intrinsic and doped a-Si:H films and a load lock unit. The separation of the chambers is required for the fabrication of high quality intrinsic films and cross-doping of n and p-type [2]. Silicon nitride films are deposited by high vacuum PECVD system, which is shown in Figure 3.2.

Figure 3.1: TUBITAK MAM ME Multi-Chamber UHV-PECVD System.

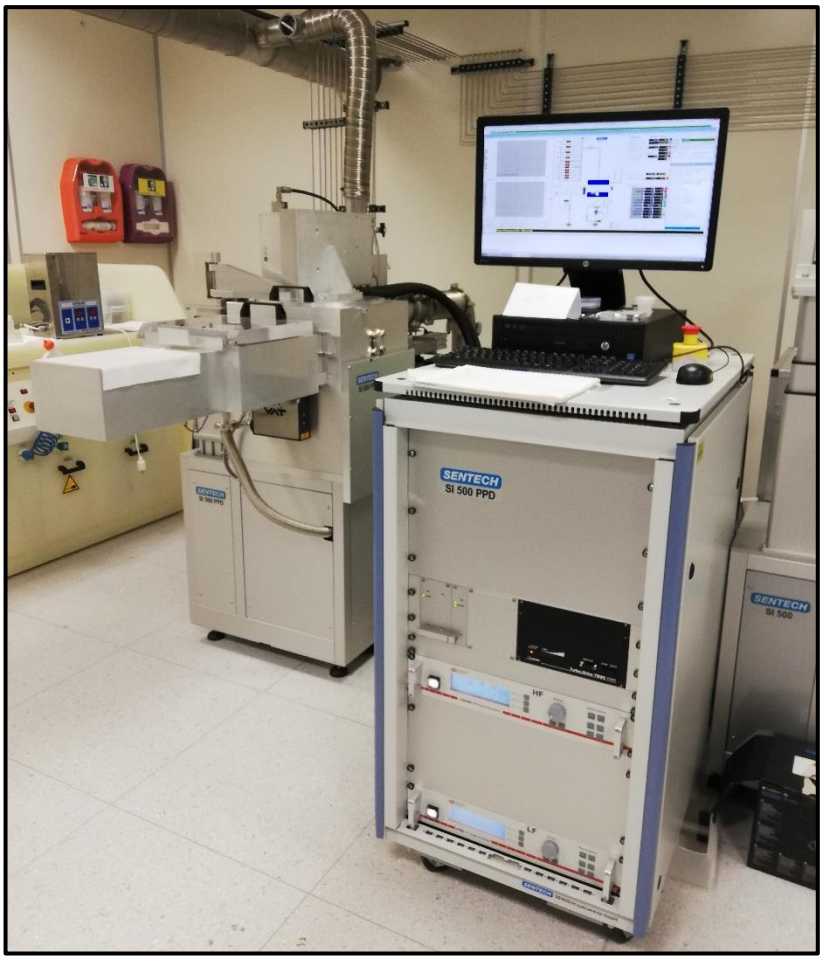

Figure 3.2: SENTECH PECVD System SI 500 PPD.

Intrinsic a-Si is used as the channel material for a-Si TFT devices in this thesis. PECVD growth of this material is performed with pure silane gas (SiH_4). Without the plasma, temperatures higher than 450°C would be required to decompose silane to form the required reactive species. At these high deposition temperatures, hydrogen is released from the a-Si, and resulting material has very high defect densities. Consequently, PECVD growth of a-Si is typically performed at around 250°C, with the plasma providing the necessary energy to decompose silane. The dominant silane decomposition reactions, which require the lowest decomposition energy, in PECVD growth are as follows [126].

$$SiH_4 \rightarrow SiH_3 + H_2 \qquad 2.2\ eV \qquad (3.1)$$

$$SiH_4 \rightarrow SiH_3 + H \qquad 4.0\ eV \qquad (3.2)$$

$$SiH_4 \rightarrow Si + 2H_2 \qquad 4.2\ eV \qquad (3.3)$$

Different other dissociation reactions are also possible during PECVD deposition of a-Si films using silane. For instance, the silane molecules can also react with the radicals produced by the dissociation reaction to form larger molecules such as Si_2H_6 and Si_3H_8, which can in turn decompose and form additional radicals [127]. Considering that the mean free path the radicals and gas molecules are on order of ~100 μm at the typical deposition pressures (0.1–1 Torr), the probability of collision and secondary reactions is very high. Consequently, it is quite difficult to clearly identify the key radicals and the associated reactions responsible for the growth of a-Si [128]. However, it is believed that SiH_3 radicals are responsible for material growth at the relatively low RF power density used during PECVD of a-Si [129]. Figure 3.3 schematically shows the process by which growth is believed to occur at the surface of a-Si via SiH_3 radical [130]. The growing surface of a-Si is usually hydrogen-terminated, and as such the SiH_3 radical is not possible directly bond to the surface. A silicon dangling bond must be provided by the release of H_2 from either incoming H radical reacting a surface H-termination or two surface H-termination reacting with each other. In that case, the SiH_3 radical is then can attach to the free silicon dangling bond and add to the growth of a-Si.

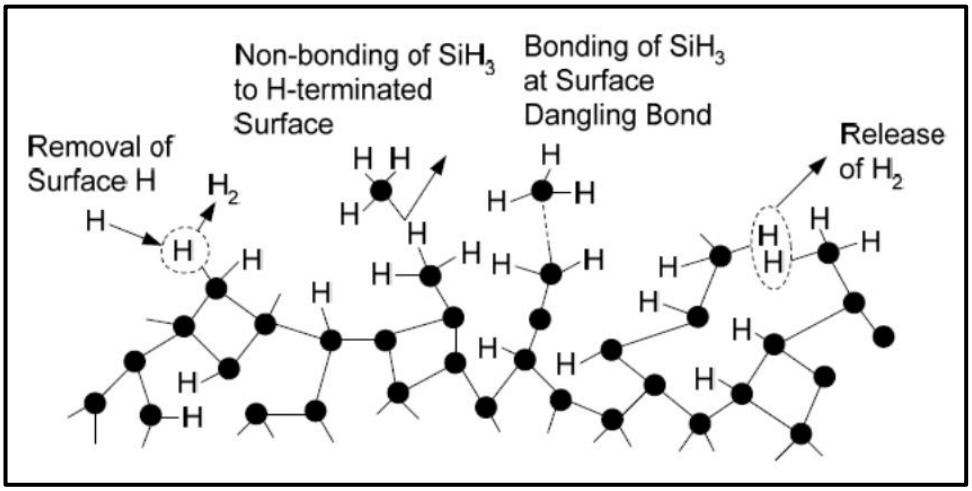

Figure 3.3: a-Si growth via SiH_3 radicals.

N-type doped a-Si is used for the source and drain contacts in a-Si TFT devices during this thesis. N-type doping of PECVD deposited a-Si is performed by adding phosphine (PH_3) to silane as precursor gas. The dopant gas molecules are dissociated by the plasma, like silane, creating reactive radicals and ions that bond to the growing surface. The typical flow ratio of the dopant gas for n^+ a-Si:H is in the few 100 ppm range.

Silicon nitride is used as the gate dielectric as well as the passivation layer for a-Si TFT devices in this thesis. The standard method of nitride film deposition for a-Si TFT device applications is PECVD. Deposition by PECVD is typically performed with a mixture of silane and ammonia. Like a-Si, PECVD SiN_x also contains a significant amount of hydrogen into its amorphous network, which again has the influence of passivating defects. In PECVD SiN_x, the ratio of nitrogen to silicon (N-to-Si ratio) may deviate from the standard 4 to 3 stoichiometric ratio depending on the deposition condition and the ratio of the precursor gases. Films with N/Si ratio higher than 1.33 are named as nitrogen-rich and films with N/Si ratio lower than 1.33 are named as silicon-rich. Figure 3.4 schematically shows the SiN_x growth mechanisms [131]. The reactions for the PECVD deposition of SiN_x are first the precursor-forming reaction as follows,

$$\mathrm{SiH_4} + 4\mathrm{NH_3} \xrightarrow{\text{plasma}} \mathrm{Si(NH_2)_3} + 4\mathrm{H_2} \tag{3.4}$$

and the next surface condensation reaction is as follows,

$$\mathrm{Si(NH_2)_3} \xrightarrow{\text{heat}} \mathrm{Si_3N_4} + 8\mathrm{NH_3} \tag{3.5}$$

The key parameters, such as the SiH_4/NH_3 ratio, RF power, substrate temperature and hydrogen dilution, influence the quality of the PECVD deposited SiN_x films.

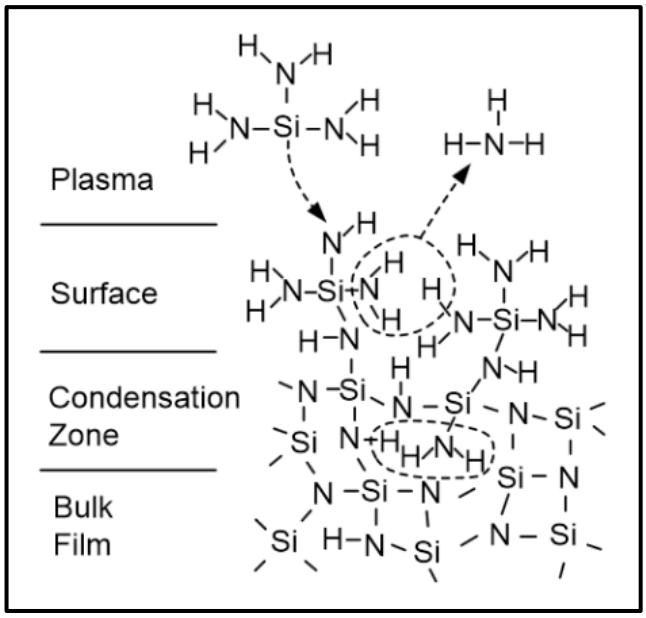

Figure 3.4: The growth mechanism of PECVD deposited SiN_x.

3.1.2. Atomic Layer Deposition (ALD)

ALD can be described as a modified version of chemical vapor deposition, where the precursors are introduced to the surface at separate cycles. During each cycle, saturation of the precursor on the surface forms and this causes a self-limiting growth. Accurate thickness control, good uniformity and perfect conformity are the main advantages of this mechanism [132].

Depositions of Al_2O_3 thin films, which are the gate dielectric of the TFT devices in this study, are performed with thermal type ALD technique. Figure 3.5 shows the ALD system where depositions are performed.

Figure 3.5: Ultratech/Cambridge NanoTech Savannah S200 ALD System.

ALD operation steps in a single cycle are: 1) Introduction of the first precursor to the chamber, 2) Purge or evacuation of chamber, 3) Introduction of the second precursor to the chamber, 4) Purge or evacuation of chamber. An amount of the material is grown on the surface after each cycle, and the specified thickness of this material is called growth per cycle (GPC) [132]. GPC does not depend on the number of the ALD cycles in most of the processes, therefore the total thickness of the film can easily be calculated by multiplying the GPC with how many times the ALD cycle is repeated. For a better understanding, ALD growth of Al_2O_3 is given in Figure 3.6.

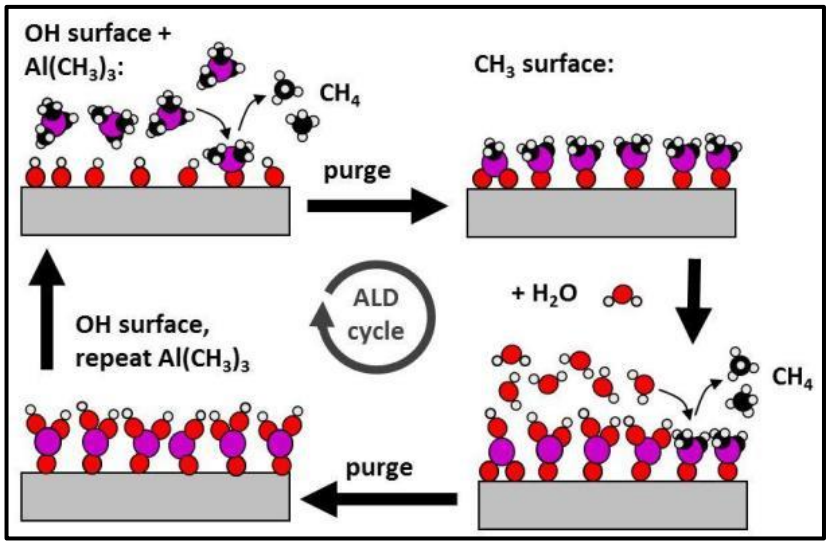

Figure 3.6: Step by step schematic illustration of one ALD cycle of Al_2O_3 growth.

Trimethylaluminum (TMA) and H_2O were utilized for Al_2O_3 growth as a precursor and reactant, respectively. The process pressure was nearly 0.2 Torr in the reactor, and the reactor was purged during the deposition with N_2 (N_2, 99.999%) at 20 sccm. N_2 was also both the carrier and purge gas. The temperature of the main chamber was maintained at 80°C during the Al_2O_3 film deposition process. Monolayer Al_2O_3 consisted of a TMA pulse for 15 ms, TMA purge for 40 s, H_2O pulse for 15 ms, and H_2O purge for 40 s in turn. This procedure was repeated 500 times (cycles) to produce an Al_2O_3 layer of nearly 50 nm thickness.

3.1.3. Metal Deposition System

Contact metallizations of a-Si TFT devices in this thesis are performed with TUBITAK MAM ME Metal Deposition System shown in Figure 3.7. This system consists of three types of deposition techniques including sputtering, thermal evaporation, and e-beam evaporation. DC magnetron sputtering method is used for deposition of Cr gate, source, and drain contact metal films.

Figure 3.7: TUBITAK MAM ME Metal Deposition System.

The main mechanism of a sputtering technique can be explained as follows: Energetic ions of the plasma formed in the reactor by the applied DC power, collides with the surface atoms of the sputtering target, and causes the scattering of the surface atoms. As a result of the scattering, the energized atoms and also the ions collide several times with the sputtering target, and the atoms sputtered from the target surface are coated to the substrate.

3.2. Thin Film Patterning Process and Equipment

Photolithography (optical lithography or UV lithography) with wet etching or dry etching is used to pattern the different transistor layers in this study.

3.2.1. Pattern Transfer by Photolithography Process

Photolithography in microfabrication process is a technique that used to transfer a pre-designed pattern from a photomask plate to a substrate. A photo-sensitive polymer, called as photoresist, is used for transferring the pattern on the photomask to the substrate. There are two main types of photoresists that differ from each other by the resulting pattern after developing process. These types are known as positive and negative modes of photoresists. A positive resist transfers an exact copy of the pattern on mask to the film, in other words, what is exposed is removed in the developer solution. On the other hand, a negative photoresist transfers an inverted mask pattern to the film, so what is not exposed is removed when developed. As soon as the photoresist is spun onto the substrate, the pattern requires to be transferred into the resist. This is performed by exposure and development processes. Exposure refers to when the photoresist is placed under an ultraviolet light source. When using a positive mode photoresist, the bonds in the exposed area are weakened. However, for a negative resist, the bonds in the exposed area are cross-linked and become stronger after exposure and a subsequent baking step. Additionally, image reversal resists can either be processed in positive or negative mode. In the positive mode, the process sequence is the same as for positive resists. In the image reversal mode, an image reversal bake after the exposure followed by a flood exposure without mask is required. After the photoresist is exposed, the

substrate is immersed in a developer bath. As a result, the developer removes the photoresist with the weaker bonds and leaves behind the desired pattern. The Figure 3.8 shows this process sequence for all the resist modes mentioned above.

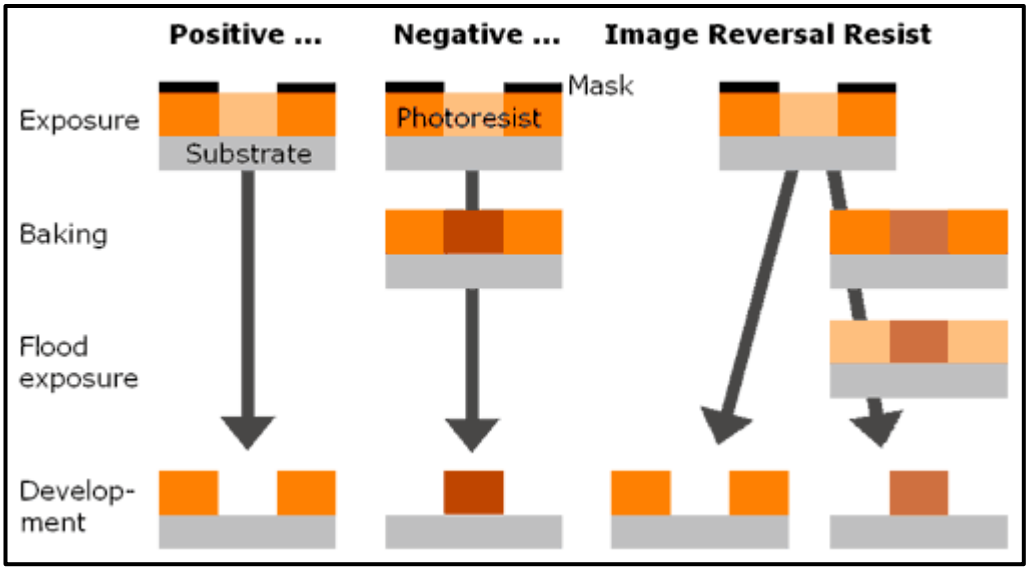

Figure 3.8: Pattern definition in positive, negative, and image reversal resists.

3.2.1.1. Alignment

In order to make useful devices, the patterns for different photolithography steps that belong to a device structure must be aligned to one another. The first pattern transferred to a substrate generally contains a set of alignment marks, which are high precision features that are used as the reference when positioning subsequent patterns to the first pattern (as shown in Figure 3.9). Alignment marks are usually included in other patterns, because the original alignment marks may be obliterated as the process progresses. It is important for each alignment mark on the substrate to be labeled so it may be identified, and for each pattern to specify the alignment mark (and the location thereof) to which it should be aligned. Since the location of the alignment mark is provided, it is easy for the operator to locate the correct feature in a short time. Each pattern of different device layers should have an alignment feature so that it may be registered to the rest of the layers.

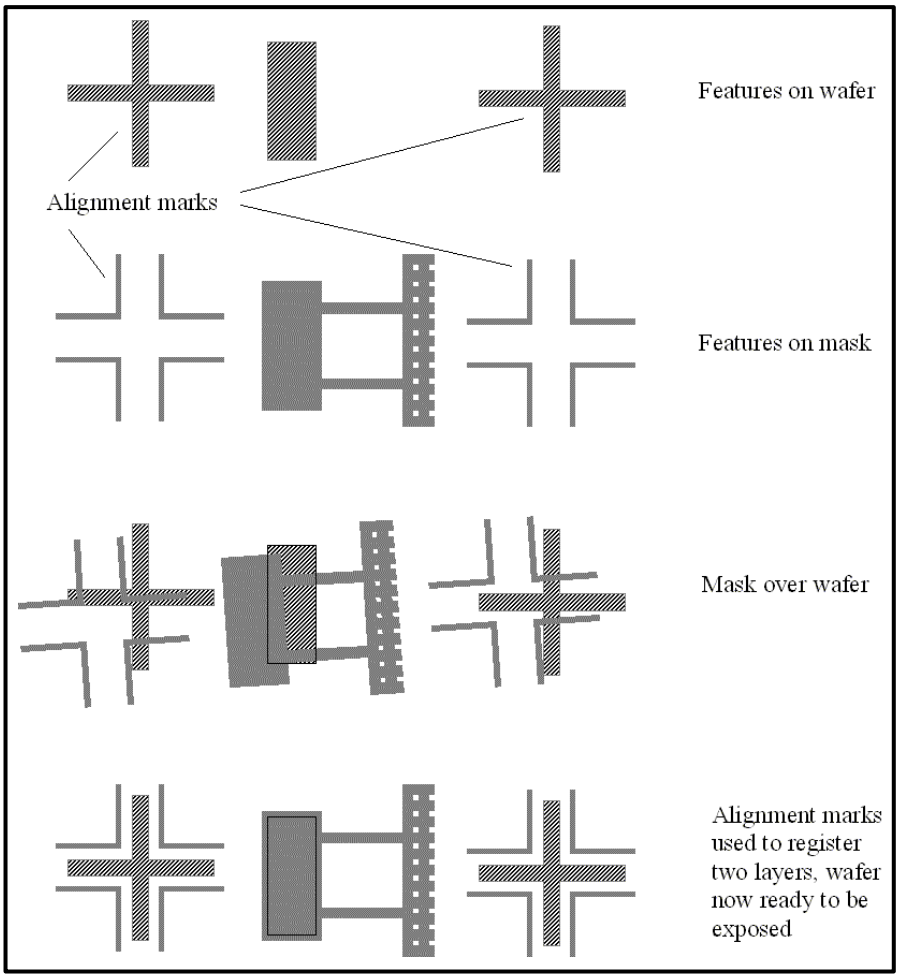

Figure 3.9: Usage of alignment marks to register subsequent layers.

3.2.1.2. Exposure

The exposure parameters required to obtain the accurate pattern transfer from the mask to the photosensitive layer depend primarily on the wavelength of the radiation source and the dose required to achieve the desired properties change of the photoresist. For different wavelengths, different photoresists exhibit different sensitivities. For good pattern transfer, the dose required per unit volume of photoresist is somewhat constant; on the other hand, the physics of the exposure process may affect the dose actually received. For instance, a highly reflective layer under the photoresist may cause the material experiencing a higher dose than if the underlying layer is absorptive, because of that the photoresist is exposed both by the incident radiation and the reflected radiation. The exposure dose also varies with the thickness of photoresist. Light is scattered and diffracted at the edges of the pattern, therefore if an image is overexposed, the dose received by photoresist at the edge that

should not be exposed may become significant. If a positive photoresist is used, this causes the photoresist image being eroded along the edges, resulting in a decrease in feature size and a loss of sharpness or corners (as shown in Figure 3.10). Moreover, if a negative resist is used, the photoresist image is dilated, causing the features to be larger than desired, again accompanied by a loss of sharpness of corners. On the other hand, if an image is severely underexposed (as shown in Figure 3.11), the pattern may not be transferred at all, and in less severe cases the results are similar to those for overexposure with the results reversed for the different polarities of resist.

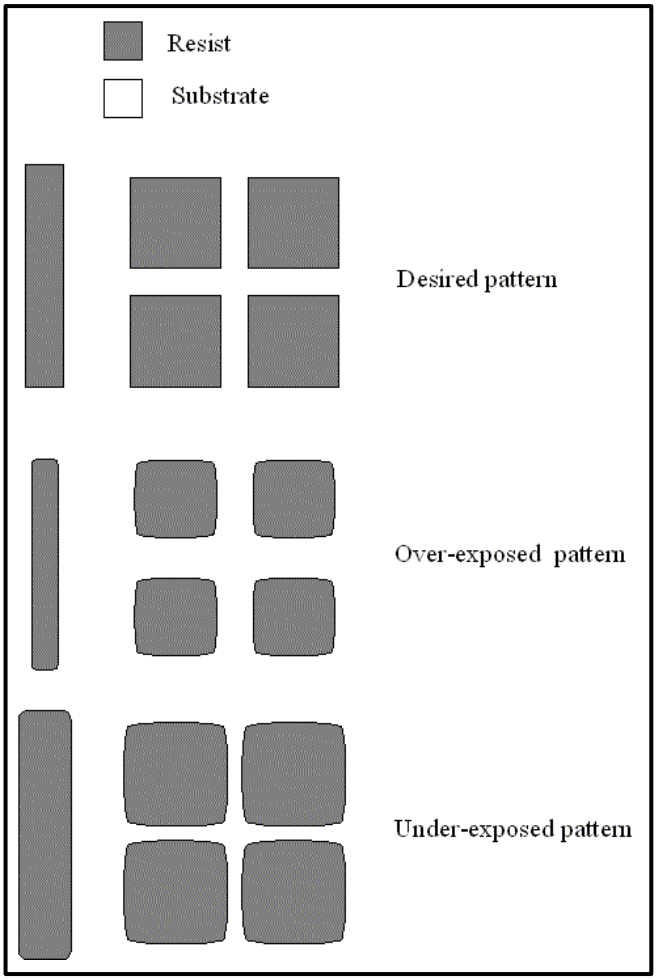

Figure 3.10: Over and under-exposure of a positive mode resist.

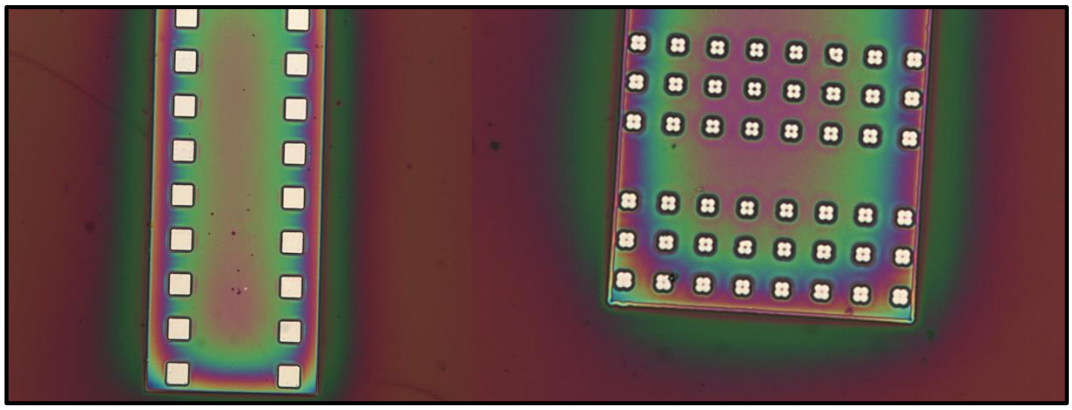

Figure 3.11: Photomicrograph of the desired pattern and under-exposed pattern for the negative mode of image reversal photoresist from our lab.

3.2.2. Etching Process

Etching can be defined as the process of removing material from a substrate. There are two main features that distinguish the etching process. These features are etched profile and selectivity. Etch profile is related to the topography of the etched film's surface and is either isotropic or anisotropic (as shown in Figure 3.12). In isotropic etching, the material is removed in all directions at an equal rate. On the other hand, anisotropic etching is the directional etching and removes the film in one direction much faster than in the other directions. Selectivity indicates how fast an etch process etches a film compared to the etch rate of a different film. There are two main etching processes: wet and dry etching.

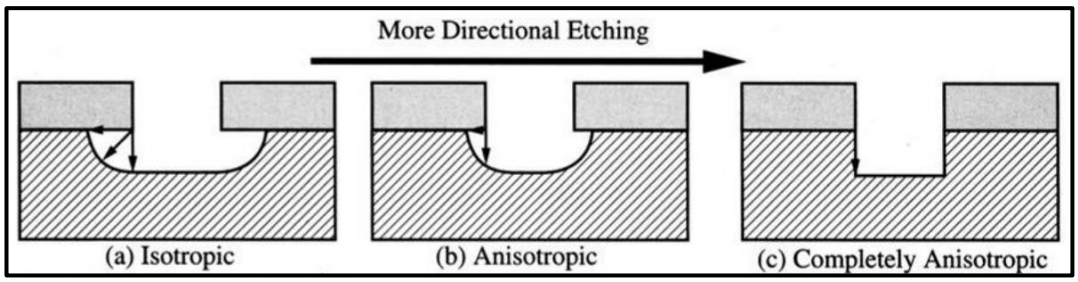

Figure 3.12: Etch profiles for (a) purely isotropic etching, (b) anisotropic etching, (c) completely anisotropic etching.

3.2.2.1. Wet Etching

A chemical etch is commonly referred to as a wet etch, as most chemical etching requires the substrate to be exposed to a liquid etchant. Compared to the physical etches, wet etches have higher selectivity, with the ability to remove one film-off of an existing film without damaging the bottom film. Chemical etches are often used to pattern devices with larger dimensions, because of that greater selectivity can be achieved compared to physical etches, and the etch chemistries typically are well understood. Since wet etches are isotropic, it limits the minimum device dimensions that can be patterned. Table 3.1 shows some materials used in thin film transistor fabrication and the appropriate wet etchants for these materials [30]. For example, silicon dioxide is generally deposited as the gate dielectric material of an electronic device, which can be etched by water-diluted HF with buffering agents such as ammonium fluoride (NH_4F). Moreover, a solution mixture of phosphoric acid, acetic acid, nitric acid, and water can be used to etch metals, such as aluminum and aluminum alloy layers, which used as the gate, source, and drain contacts in TFT devices.

Table 3.1: Suitable wet etchants for some materials.

Material	**Etchant**
SiO_2	NH_4F-HF (7:1) BHF, 35°C
SiO_2 (on MoW)	(NH_4F-HF)-H_2O (1:20)
Al	H_3PO_4-HNO_3-H_2O (80:4:16)
Mo	H_3PO_4-HNO_3-H_2O (80:4:16)
Cr	HNO_3-H_2O (1:1)
Ni	HNO_3-CH_3COOH-H_2SO_4 (5:5:2)
Ti	HF-H_2O_2
MoW	$Na_2S_2O_{3(sat\ aq)}$-$K_2S_2O_5$ (50 ml $Na_2S_2O_3$, 1 g $K_2S_2O_5$)

3.2.2.2. Dry Etching

The physical etching, or dry etching as it is called in general, is performed in a plasma source under high controllability of process parameters. And there is also the interdependence between etching parameters and plasma properties. A physical etch is an anisotropic etch, as etch is directed in one direction. The basic operation principle of the dry etching depends on the chemical and physical interaction of the layer to be etched with the etchant chemical gases. Usage of the plasma (due to the highly directional ions) makes this etching a highly anisotropic type. Because of its better directionality, more reliability, and less environmental impact, dry etching can be preferable against wet etching. However, poor selectivity is a disadvantage of physical etch. The main plasma sources used for dry etching vary depending on the type of energy transfer to the electrons, and these sources include the capacitively coupled plasmas (CCP), inductively coupled plasmas (ICP), electron cyclotron resonance (ECR), surface wave plasmas (SWP), and helicon wave plasmas (HWP). In TFT fabrication processing, especially in industry, CCP is often used because of the easier control of the etch uniformity. However, due to their ability to etch on substrates larger than 1 m^2 with high etching rates and low damage, ICP sources as a plasma source in dry etch technique are dominant compared to the CCP.

Process comparisons between wet and dry etch techniques are given in Table 3.2 [30].

Table 3.2: Comparisons between wet and dry etch process.

	Wet etching	**Dry etching**
Etching rate	High	Low
Uniformity	Poor	Good
Repeatability	Poor	Good
Critical dimension loss	Large	Small
Selectivity to under layer	Good	Poor
Profile control	Very poor	Good
Multilayer etch	Difficult	Possible
Advantage	High selectivity	Anisotropic
	Free of damage	Fine-pattern definition
	High throughput	Fewer waste problems
		Better process control
Disadvantage	Isotropic	Damage issue
	Fine-pattern limitation	Selectivity issue
	Incomplete etching	Low throughput
	Bubble formation	
	Scum remainder	
	Adhesion-problem	

3.2.3. The Photolithography Module

Patterning steps of all of the layers of the TFT devices are carried out with using photolithography. A typical photolithography process flow using etching technique is demonstrated in Figure 3.13. The main steps of the photolithography are as follows:

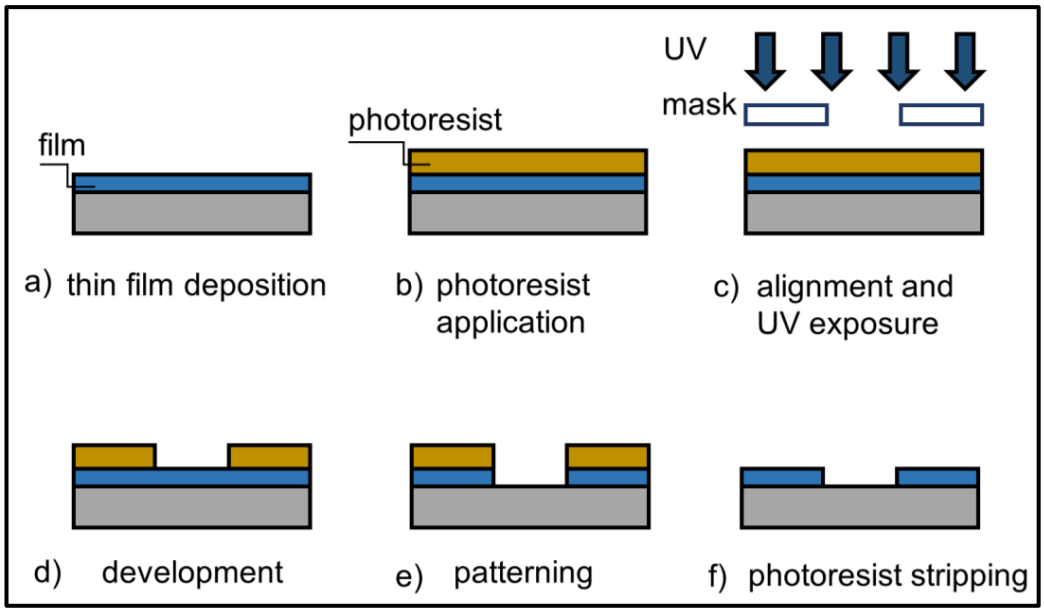

Figure 3.13: Photolithography process and thin film patterning using etching technique.

1) General cleaning of the substrate: This step includes the solvent cleaning for the removal of the possible organic contamination or dust particles at the substrate surface. The substrate is cleaned using acetone, isopropanol (IPA), and DI water, respectively, then dried with the nitrogen gas.

2) De-hydration step: This step includes the vaporization of the possible water droplets on the substrate surface. The sample is placed on the surface of a hot plate which higher than the evaporation temperature of the water, and the temperature of which is kept at 110°C.

3) Photoresist application: After the vaporization step, the photoresist is coated on the substrate surface (on top of the thin film deposited on the substrate). However, before the photoresist coating, it is generally preferred to coat a chemical called Bis (trimethylsilyl) amine (HMDS) as an adhesion layer. In this study, the photoresist application is performed in a spin coater system shown in Figure 3.14. The thickness of the photoresist is a parameter that depends on the spin speed and viscosity of the photoresist. AZ 5214E and AZ 1505 are used as the photoresists in the studies of this thesis. The photoresist processing parameters are given in Table 3.3.

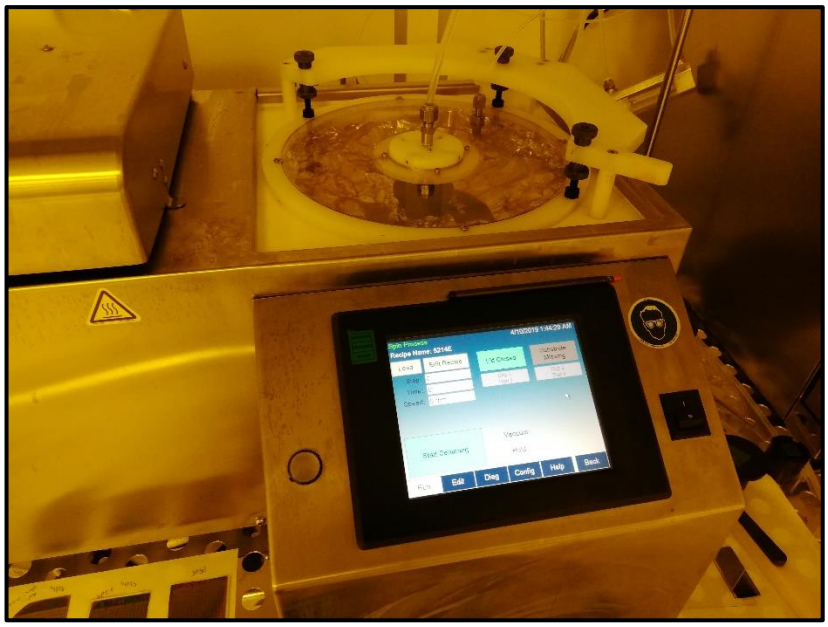

Figure 3.14: CEE Brewer Science Model 200CBX Spin Coater.

Table 3.3: Processing parameters for the photoresists used in this study.

Photoresist	**AZ 1505**	**AZ 5214E**
Photoresist type	Positive	Image reversal
Spin speed [rpm]	4000	4000
Photoresist thickness [µm]	0.5	1.4
Prebake temperature [°C]	100	110
Exposure dose [mJ cm^{-2}]	100	160
Developer	AZ 726 MIF	AZ 351B
Postbake temperature [°C]	110	120

Note that processing parameters given in Table 8 for AZ 5214E is for its positive mode. These parameter values are also valid for the negative mode of AZ 5214E excluding exposure dose, and also there are two extra process steps in its negative mode application: after exposure of 60 mJ cm^{-2}, an image reversal bake (120 °C / 120 s) and a flood exposure (200 mJ cm^{-2}), respectively.

4) Prebake (or Softbake) step: This step is performed to drive off the excess photoresist solvent from the substrate surface. The photoresist coated sample is placed in a hot plate for typically 60 seconds. The surface temperature of its depends on the photoresist used.

5) Alignment and Exposure: Contact aligner is used to align the substrate and the photomask. After alignment, the photoresist coated sample is exposed to ultraviolet light in hard contact mode, in which the substrate is brought in direct contact with the mask. The UV exposure dose changes with the photoresist used. The mask alignment and exposure process are performed in a mask aligner system shown in Figure 3.15, equipped with a 350 W mercury arc lamp UV source.

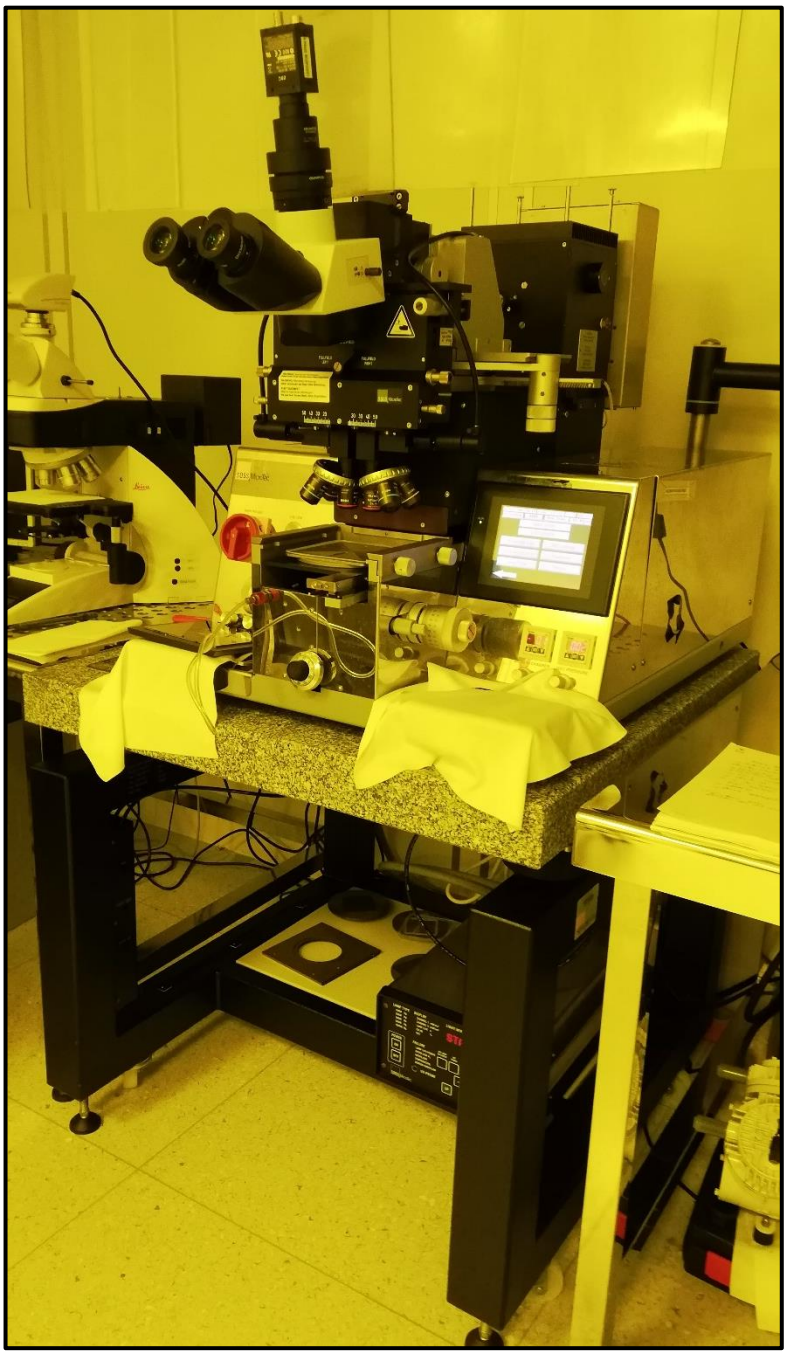

Figure 3.15: SUSS MicroTec MJB4 Manual Mask Aligner System.

For a positive mode photoresist: In this step, some parts of the photoresist coated substrate are protected from the UV light by a photomask. After the UV light exposure of the sample, the photoactive compound of the photoresist becomes dissolvable in a chemical solution called the developer. For a photoresist in negative mode, the reverse of this process is valid.

6) Development step: The development of the photoresist is performed by the immersing of the photoresist coated sample to the developer solution. In the development process, AZ 726 MIF developer for about 20–40 seconds is used for AZ 5214E photoresist. On the other hand, the chemical solution consisting of AZ 351B:H_2O (1:4) for about 60–80 seconds is used for AZ 1505 photoresist. If a photoresist in positive mode is used, the UV exposed part of the sample will be removed. However, the non-exposed part of the sample will be removed for a negative photoresist application.

7) Postbake (or Hardbake) step: To increase the stickiness of the photoresist to the substrate surface, the sample is placed in a hot plate for a period ranging from 3 to 10 minutes. The surface temperature of its depends on the photoresist used.

8) Patterning: The non-photoresist-coated thin film is removed by a chemical solution (wet etching) or plasma (dry etching). Wet etching (chemical etching) technique is used to pattern Cr gate, source, and drain metal contacts. These layers are etched using Cr etchant which is a mixture of perchloric acid ($HClO_4$) and ceric ammonium nitrate $(NH_4)_2[Ce(NO_3)_6]$. The active channel layers and the dielectric layers of the devices are etched by the dry etching method. The etching processes of these layers are performed in an Inductively Coupled Plasma-Reactive Ion Etcher (ICP-RIE) system shown in Figure 3.16.

Figure 3.16: SENTECH ICP-RIE Plasma Etching System SI 500.

9) Photoresist stripping: After patterning the film, the remaining photoresist is removed using an organic solvent. The photoresist stripping process is performed using AZ 100 Remover stripper.

3.3. TFT Electrical Characterization

The current-voltage (I-V) measurements are performed using a semiconductor characterization system (Keithley 4200-SCS) and a probe station. Figure 3.17 shows the schematic diagram of this characterization equipment. The micro-probe tips have 10 microns in diameter.

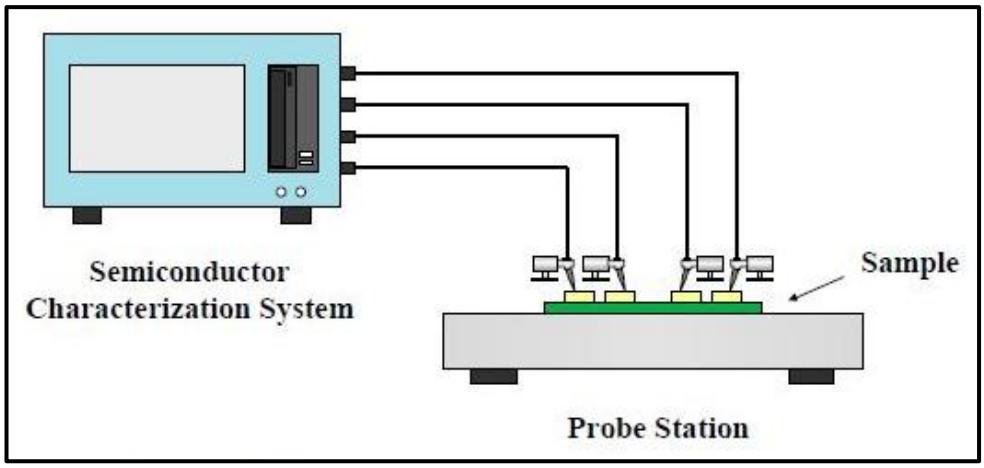

Figure 3.17: Schematic diagram of the characterization system.

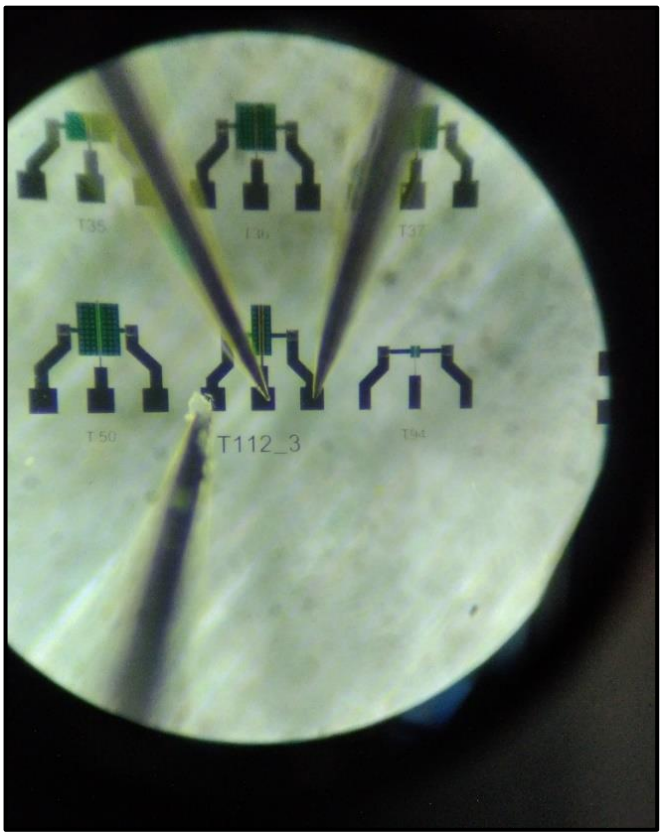

Figure 3.18: Electrical measurement of one of TFTs on the sample (probes on the source, drain, and gate contacts -from left to right-).

I-V characteristics of the TFT devices are obtained as follows: 1) A constant gate bias voltage is applied. 2) The voltage difference between the drain and source contacts is swept. 3) Step 2 is repeated under different gate bias voltage conditions, and the so called family of curves is obtained.

4. RESULTS and DISCUSSION

This chapter presents the outputs of this study, which consist of the fabrication and characterization of the devices. The first part of the chapter provides the fabrication details of all the fabricated TFTs, and the second part includes the electrical characterization of the devices.

4.1. Device Fabrication

Device fabrication consists of two main parts: fabrication of top-gate thin-film transistors and fabrication of bottom-gate thin-film transistors. Top gate process requires 9 thin film depositions, and 6 lithography processes and therefore 6 masks are used for top-gate TFT fabrication. On the other hand, the bottom gate process requires 8 thin film depositions, and 5 lithography processes and so 5 masks are used for bottom-gate TFT fabrication. 5" Chromium mask sets used for fabrication of top-gate and bottom-gate devices are shown in Figure 4.1 and 4.2. Each step in TFT fabrication for both device structures is described as follows.

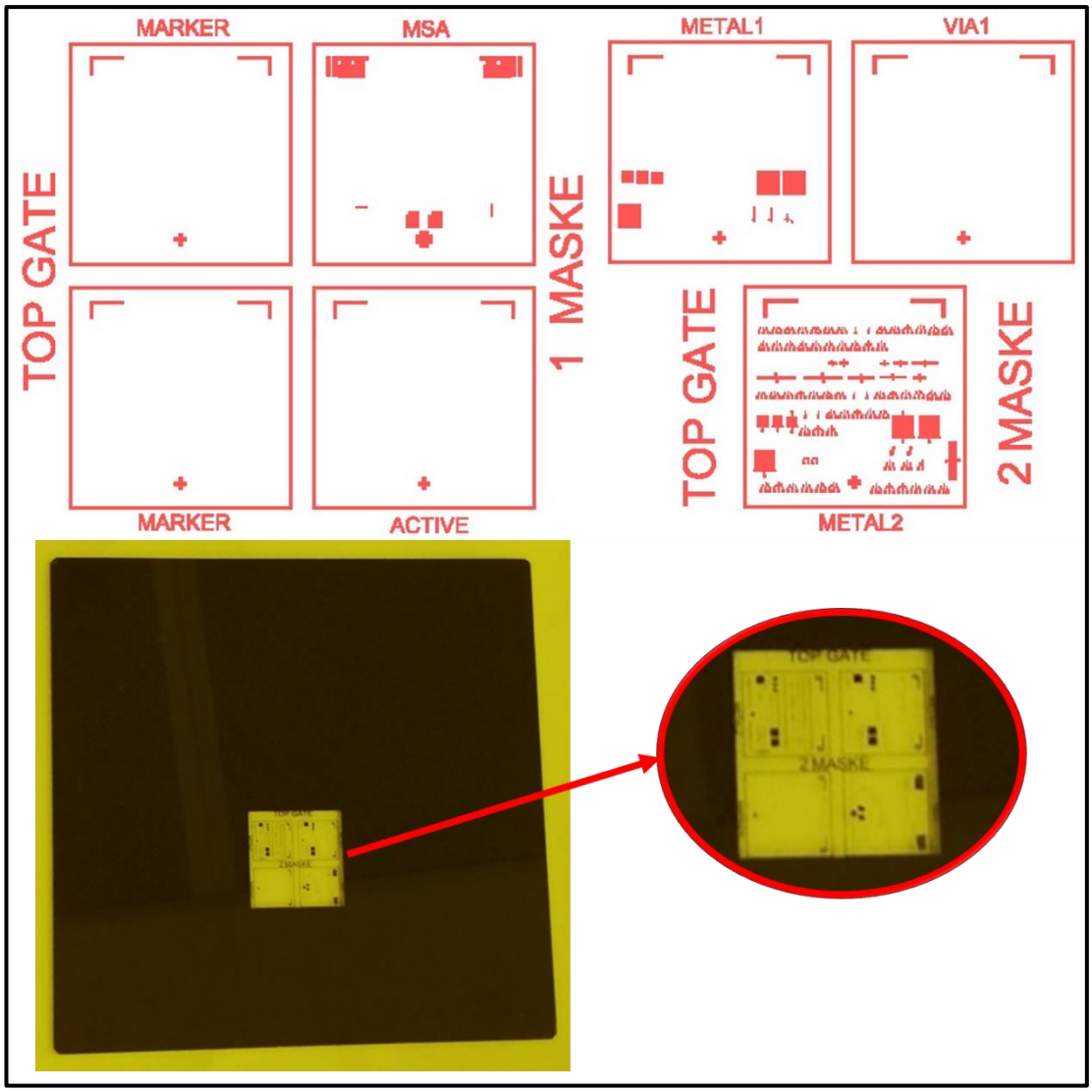

Figure 4.1: Computer drawings and images of mask set used in the fabrication of top-gate TFTs (mask set includes lithography steps which are Marker, Mesa, Active, Metal 1, Via, and Metal 2, respectively).

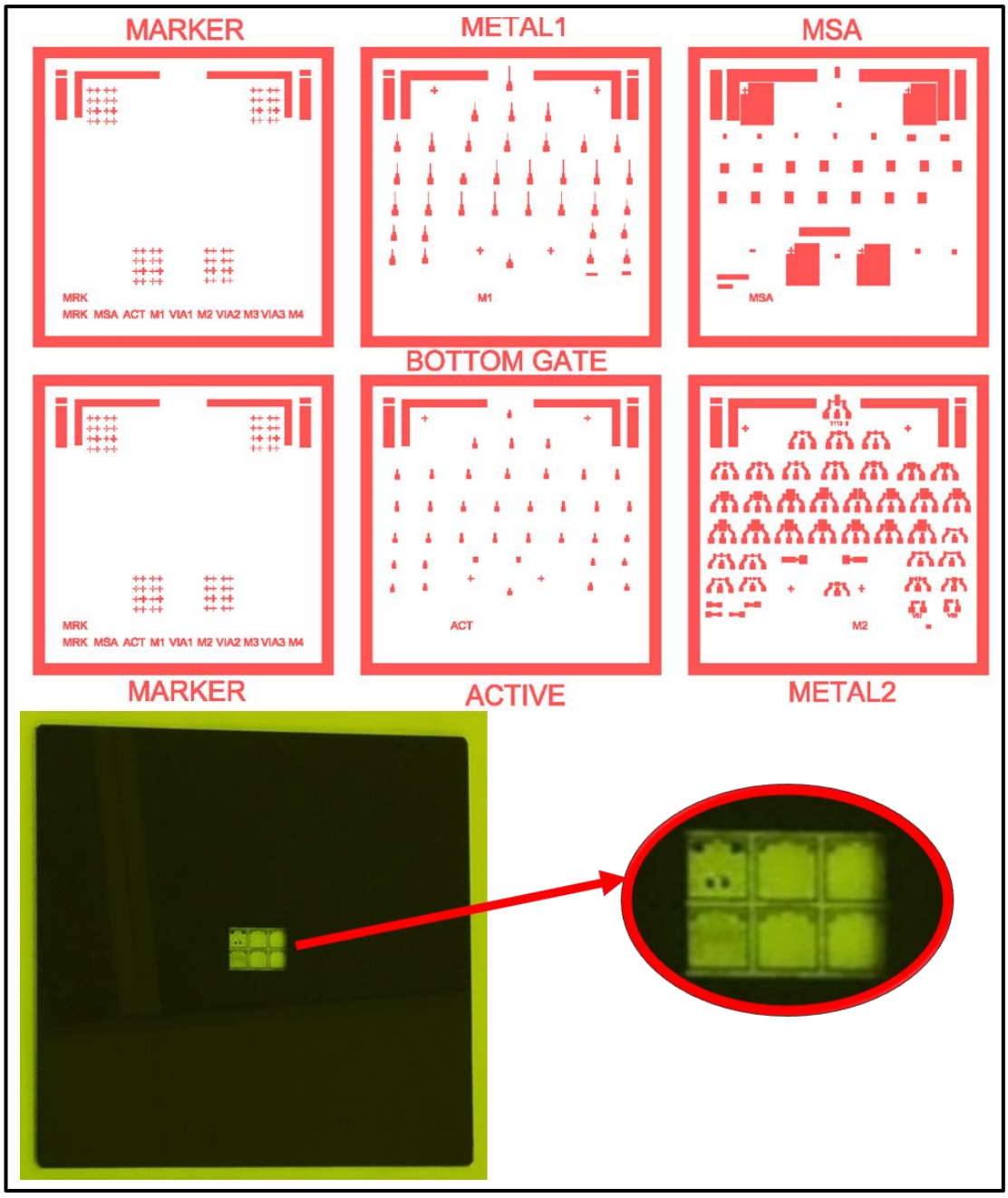

Figure 4.2: Computer drawings and images of mask set used in the fabrication of bottom-gate TFTs (mask set includes lithography steps which are Marker, Metal 1, Mesa, Active, and Metal 2, respectively).

4.1.1. Top-Gate Thin-Film Transistors (TG-TFTs)

a-Si:H TFTs are fabricated on glass substrates in top-gate configuration. Device fabrication steps are described as follows.

1) Substrate preparation: Corning Eagle XG 2" square glass substrates are prepared for fabrication process with chemical cleaning process in the literature. Cleaning methods used in this study are given in Table 4.1 [133]. In order to remove organic and inorganic contamination on the substrate surface, the following glass cleaning process is carried out. In order to remove organic contaminations, glass substrates are cleaned using Method 1. Then, substrates are cleaned using Method 2 to remove inorganic contaminations.

Table 4.1: Chemical cleaning methods of glass substrates used in this study.

Method	Steps
1	30 min in 1:1 MeOH:HCl
2	Method 1 + additional incubation (30 min) in conc. H_2SO_4 Rinse in H_2O, dry under N_2

2) Deposition of a-Si:H films and Marker lithography: As shown in Figure 4.3 (a), intrinsic a-Si:H and n-type doped a-Si:H layers were deposited with PECVD on the glass substrate. According to the deposition rates, the total thickness of the two layers is 460 nm and one-third of this is n-doped layer. Then, Cr metal was deposited on the whole surface by the DC magnetron sputtering method. AZ 1505 photoresist was used in Marker lithography. After deposition of marker metal, pattern transfer of marker metal was performed with thin photoresist, and the first lithography step was completed with Cr Etcher. Metal markers are shown in Figure 4.3 (b).

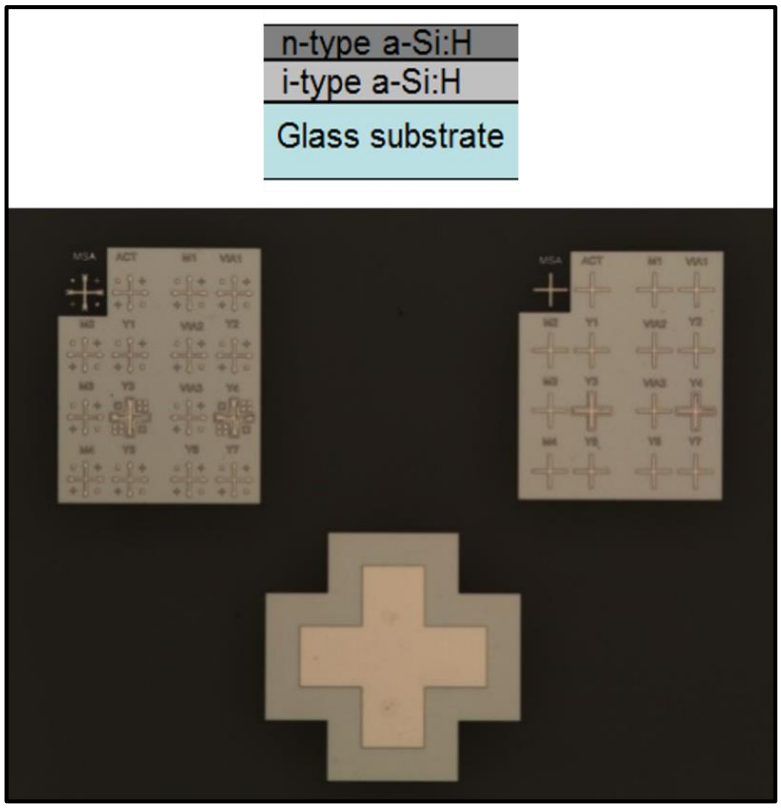

Figure 4.3: (a) schematic cross-sectional view of active layers deposited on glass, (b) photomicrograph of markers.

3) Mesa lithography and definition of TFT island: Mesa lithography of a-Si:H layers was performed with Mesa mask. In this lithography step, AZ 5214E photoresist, which is about 1.5 microns thick and is more resistant to the etch process, was used with the image reversal method. After lithography, i.e. before etching, heat processing by hot plate was carried out at 110°C for 15 minutes. Then, dry etch process by ICP-RIE system with CF_4/H_2 plasmas up to glass layer (depth of 460 nm) and removal of the remaining photoresist by heated remover (60°C) were performed. Thus, the active layers of the devices were separated from each other by mesa isolation. Figure 4.4 shows a-Si:H islands on the glass, where TFTs will be placed.

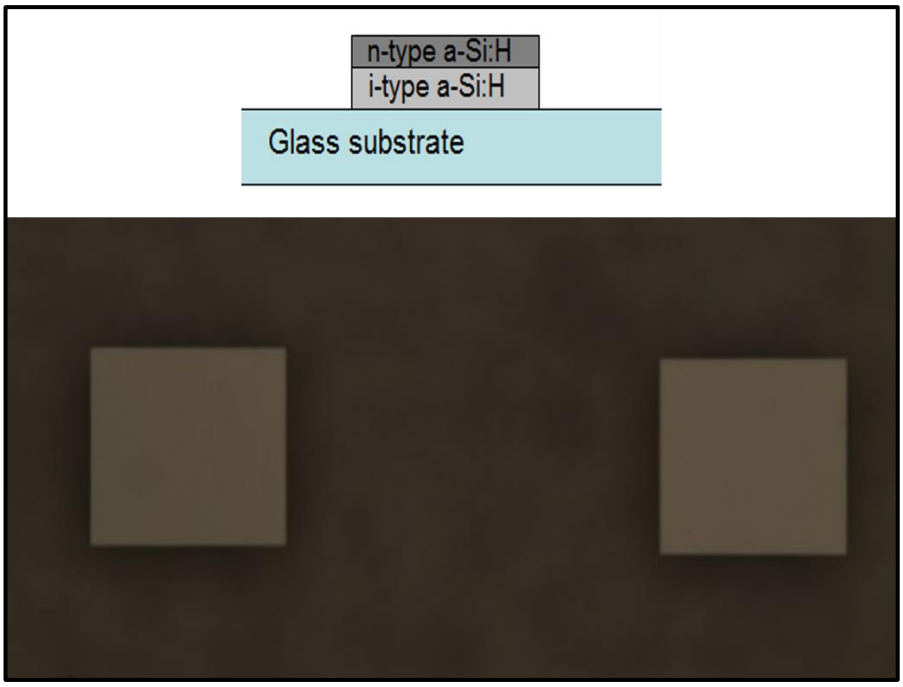

Figure 4.4: Schematic cross-sectional view and photomicrograph of the island (active device area).

4) Deposition of passivation layer and Active lithography: Deposition of 50 nm SiN_x layer was performed with PECVD system. Then, contact windows opening process with dry etching for source and drain metal layers was carried out in ICP-RIE system with CF_4/H_2 plasmas as the same, at which stage approximately 60 nm etching was performed. Figure 4.5 shows the TFT device after dry etching and immersion in AZ 100 Remover (60°C) for 30 minutes and ultrasonic bath for 15 seconds.

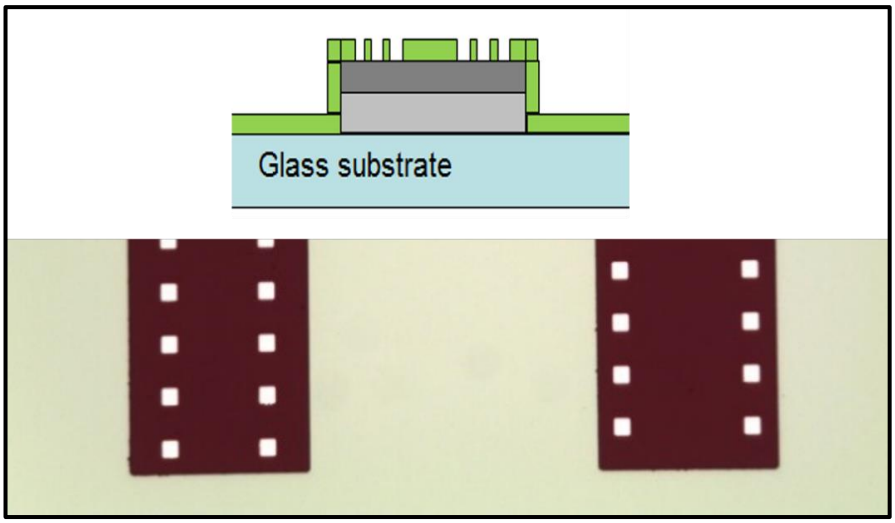

Figure 4.5: Schematic cross-sectional view and photomicrograph of device after passivation layer deposition and contact window opening process.

5) Metal 1 lithography: For metal contacts, first Cr metal with a thickness of 150–200 nm was deposited on the whole sample by the sputtering method. What is important in this process is the full deposition of metal interconnects (source and drain) on the sidewalls of mesa structures. After metal deposition, the sample was prepared for Cr wet etching using M1 mask and AZ 1505 resist. In wet etching, Cr etcher solution was used at 30°C, and it makes 100 nm wet etching per minute. Schematic of the device after these processes are shown in Figure 4.6 (a). Figure 4.6 (b) shows the optical microscope image of the TFT after applying M1 mask and lift-off process.

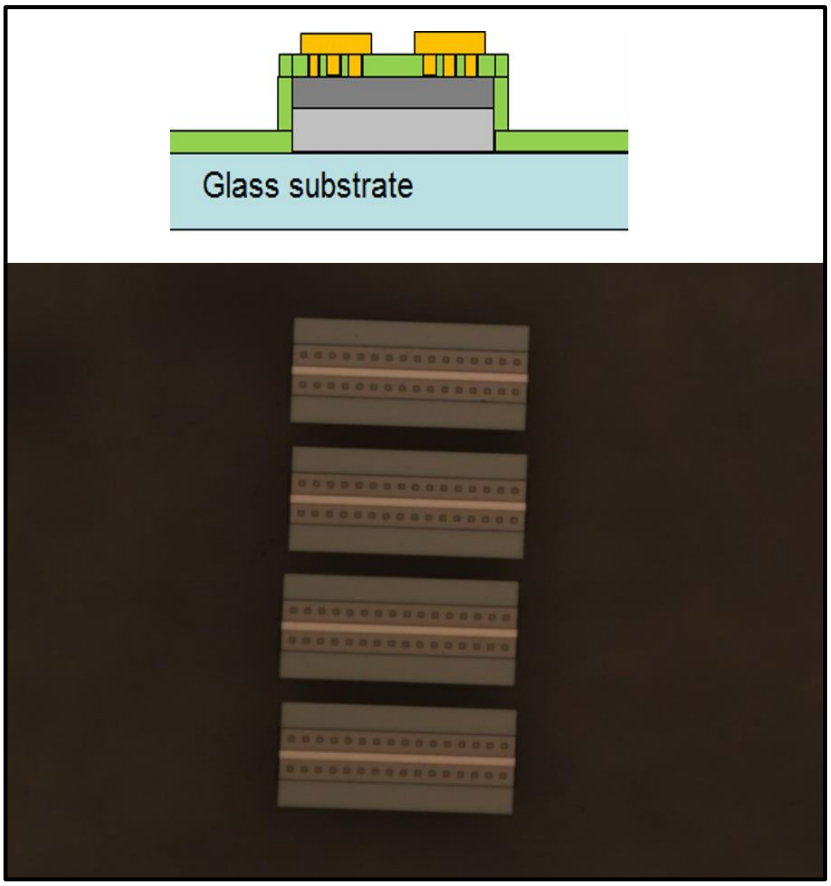

Figure 4.6: (a) source and drain metal contacts, (b) etching of the n-type layer after metal deposition.

6) Formation of the channel region by ICP-RIE dry etching process: In this step, self-alignment was applied by using M1 metal as a dry etching mask. It is planned to reach the channel layer by etching 50 nm SiN_x and 154 nm n^+ a-Si:H layers in TFT by the dry etching process. In Figure 4.7 (a), the configuration of the TFT device is schematized. Figure 4.7 (b) shows the actual TFT device after etching. In this etching, it was reached deeper than expected. In this figure, the gate length is 5 microns.

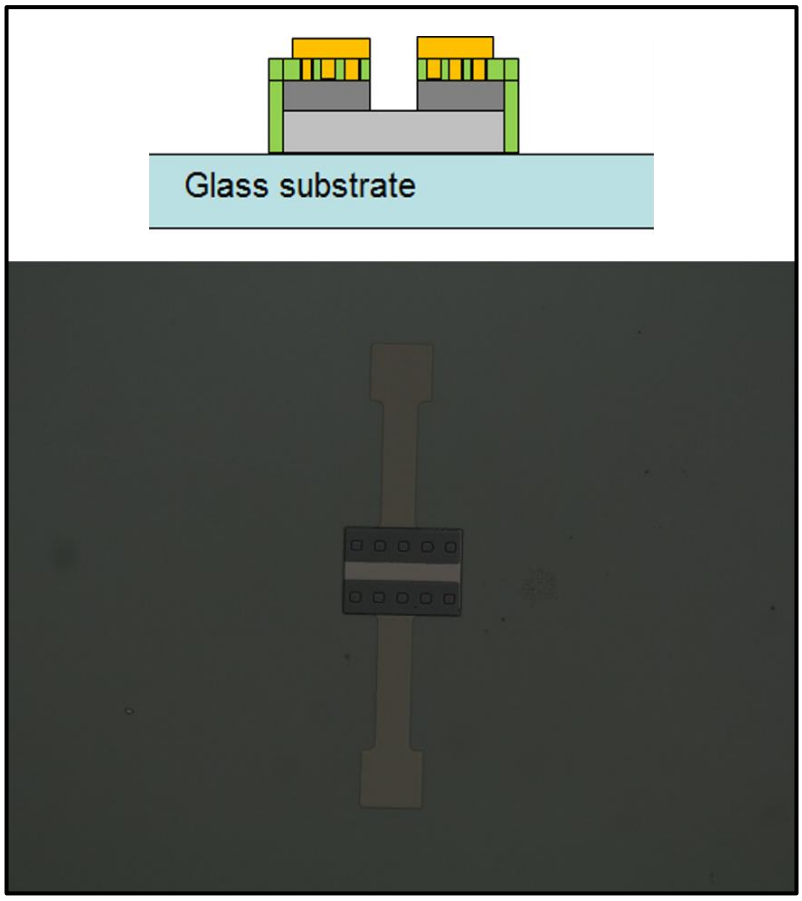

Figure 4.7: (a) schematic cross-sectional view of channel, (b) removal of the passivation SiN_x and n^+ a-Si:H layers by the dry etching process.

7) Deposition of gate dielectric layers and Via lithography: In this step, about 50 nm Al_2O_3 and 200 nm SiN_x deposition with ALD and PECVD, respectively and opening the windows for the next step which is M2 metal deposition by using Via mask are performed. Figure 4.8 (a) illustrates schematic of TFT structure after Al_2O_3 and SiN_x deposition (bilayer gate dielectric), and also Figure 4.8 (b) illustrates configuration schematically after the dry etching process. In this lithography, AZ 5214E was used as photoresist. For dry etching of Al_2O_3 layer, ICP-RIE system with BCl_3/Ar plasmas was used. Figure 4.8 (c) shows the optical image of the TFT device after opening the windows with the Via mask.

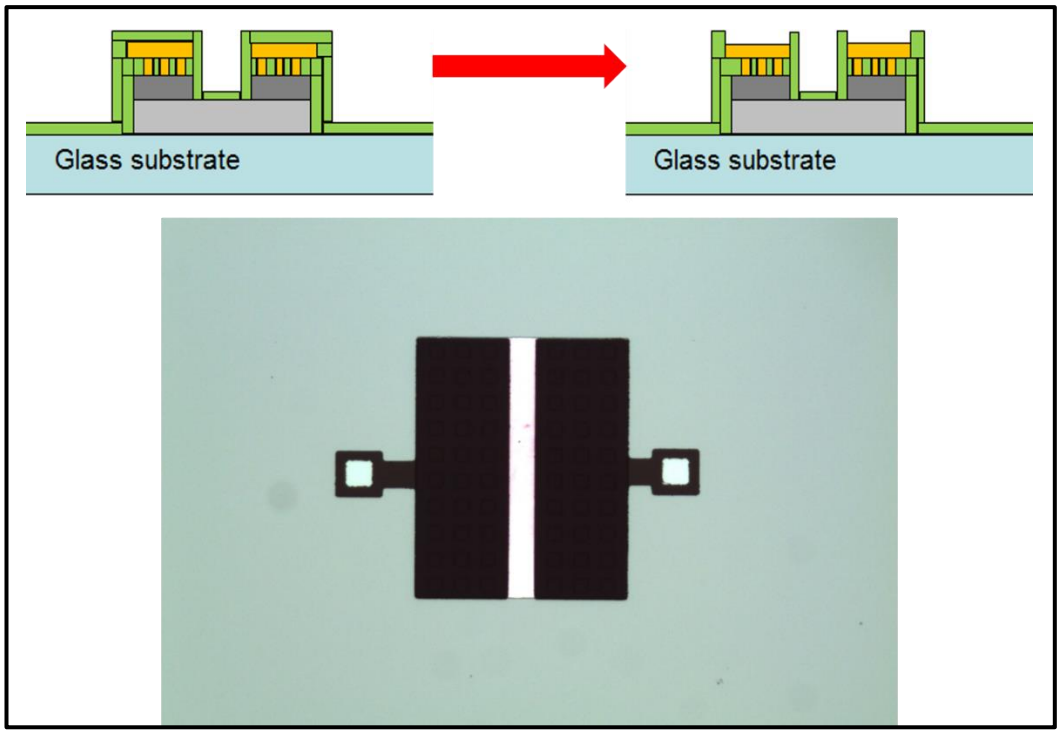

Figure 4.8: Schematic cross-sectional view of (a) bilayer gate dielectrics and (b) Via, (c) deposition of gate dielectric layers and opening the windows with the Via mask.

8) Deposition and patterning (Metal 2 lithography) of source, drain, and gate metal layers: In this step, about 150 nm Cr metal was deposited with Sputter system on the whole surface. The future places of source, drain, and gate electrodes were determined with AZ 1505 resist. The wet etching was carried out with Cr etcher at 30°C as the same. After this process, microfabrication was completed with the several heat processing performed in the annealing furnace. Schematic cross-sectional view and photomicrograph of the final device are shown in Figure 4.9. In Figure 4.9 (b), the gate length is 10 microns. Figure 4.10 shows the photo of the final sample.

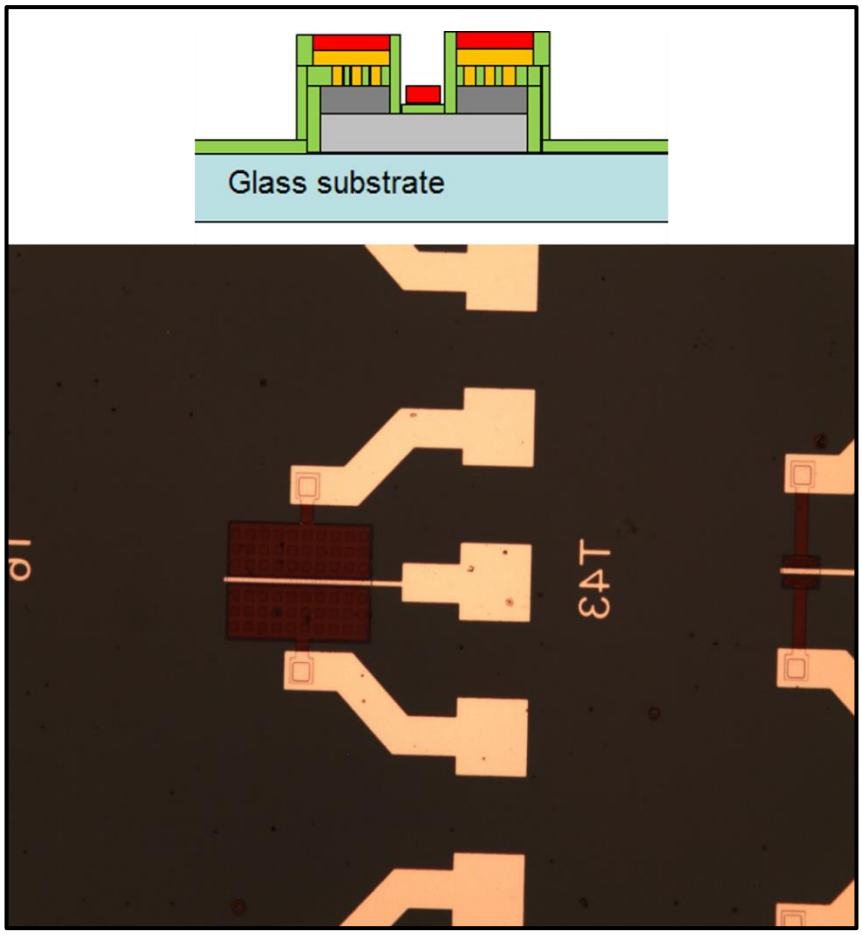

Figure 4.9: Deposition of source, drain and gate metals by using M2 mask.

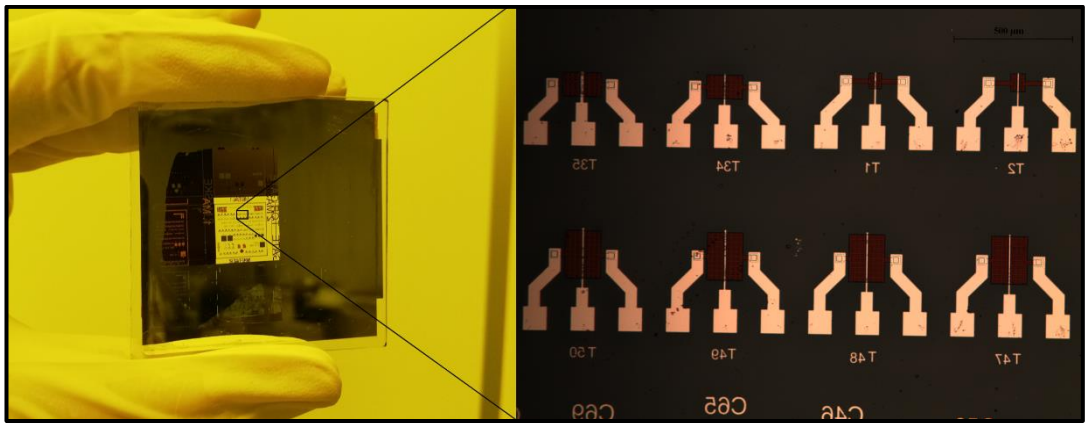

Figure 4.10: (a) the fabricated sample, (b) the TFT array on the glass substrate.

4.1.2. Bottom-Gate Thin-Film Transistors (BG-TFTs)

a-Si:H TFTs with bottom-gate configuration are fabricated on glass substrates. TFT fabrication steps are described as follows. Preparing of glass substrates with the cleaning process for the bottom-gate TFT fabrication process is the same as the substrate preparation for the top-gate TFT fabrication as described above.

1) Marker lithography and gate metal deposition & patterning: Firstly, thin 50 nm SiN_x was deposited on the glass substrate. The performed processes are the same for both the Marker and Metal 1 lithography steps, which are the 1st and 2nd steps respectively. 100–150 nm thickness of Cr is deposited by Sputter system for markers and gate metal. The sample was prepared for Cr wet etching using AZ 1505 resist. The Cr etcher solution was used at 30°C for wet etching and wet etching is performed at 100 nm per minute. Figure 4.11 shows the optical microscope image of the device after wet Cr etching in Metal 1 step and deposition of all thin film layers.

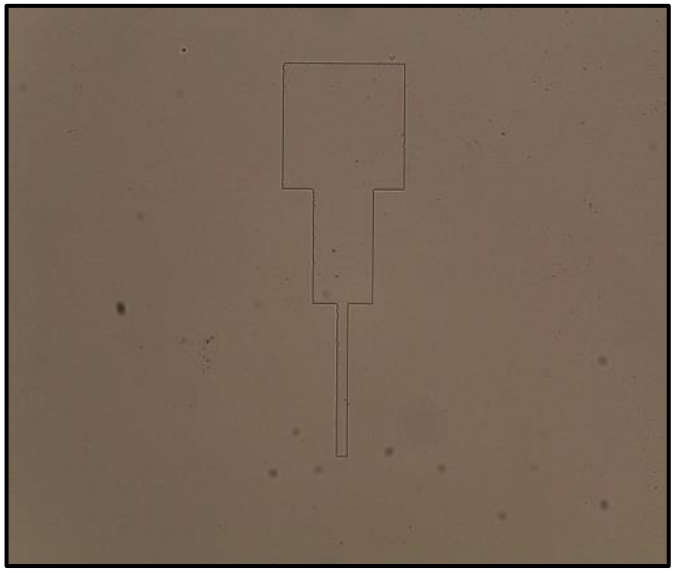

Figure 4.11: Photomicrograph of the gate metal (the image was taken after M1 deposition and deposition of SiN_x/Al_2O_3 -bilayer gate dielectric-, and amorphous silicon layers).

2) Mesa lithography with dry etching process: Mesa lithography of the a-Si:H layers was performed with Mesa mask. In this step, AZ 5214E was used as photoresist, this resist is about 1.5 microns thickness and more resistant to the etching process. After

the mesa pattern transfer, heat processing of sample was performed with the hot plate at 110°C for 15 minutes. Then, dry etching of SiN_x and a-Si:H layers by CF_4/H_2 plasmas and Al_2O_3 layer by BCl_3 with ICP-RIE system up to glass layer (depth of 460 nm) and removal of the remaining photoresist by heated remover (60°C) were performed. Thus, the active layers of the devices are separated from each other by mesa isolation. The image of the device after the mesa step and the resist stripping process is shown in Figure 4.12.

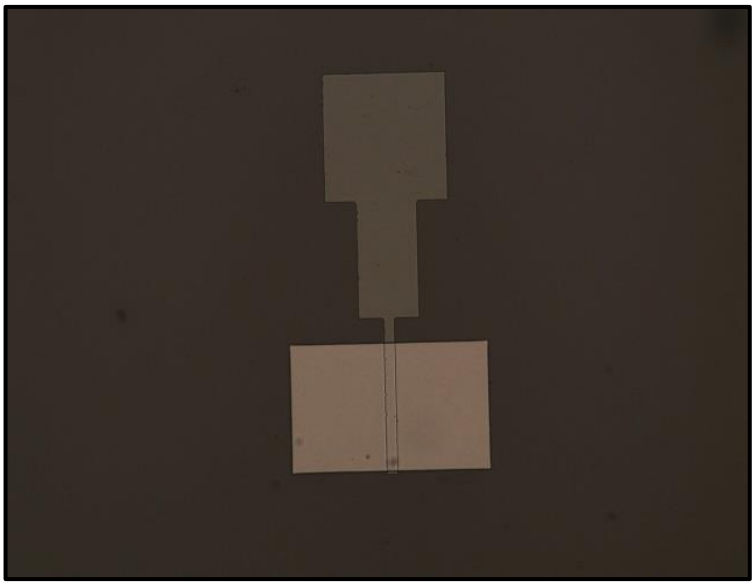

Figure 4.12: Photomicrograph of the TFT device after Mesa lithography.

3) Deposition of passivation layer and Active lithography: In this step, 50 nm thickness SiN_x was deposited by PECVD, and then with Via mask, parts, where metals will be deposited, was opened by dry etching up to n-doped amorphous silicon. The microscope image of the device after via step is shown in Figure 4.13.

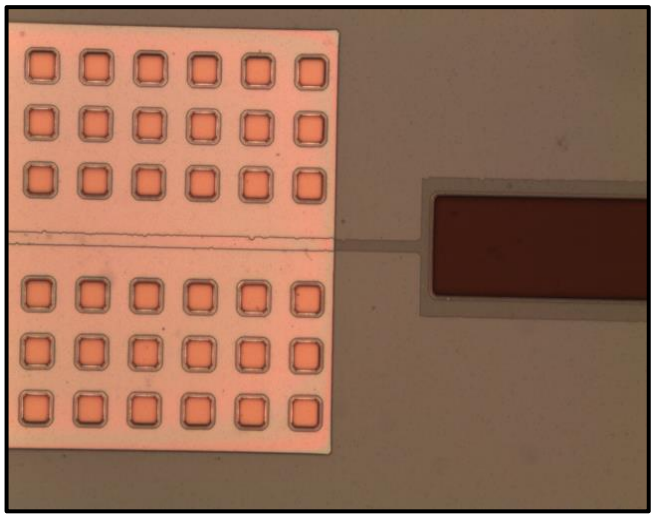

Figure 4.13: Photomicrograph of the TFT device after Via lithography (the opened windows -via- are 20 microns in size).

4) Metal 2 lithography: In this step, about 150 nm Cr metal was deposited by the sputtering method to the whole surface of the sample. The future places of source, drain, and gate electrodes were determined with AZ 1505 photoresist. The wet etching was carried out with Cr etcher at 30°C as the same. After this process, microfabrication was completed with several heat processing in the annealing furnace. The microscope image of the device is shown in Figure 4.14 (a). Figure 4.14 (b) shows the schematic of the device in cross-section. In this step, sometimes the lift-off method was also used. The photo of the final sample is shown in Figure 4.15.

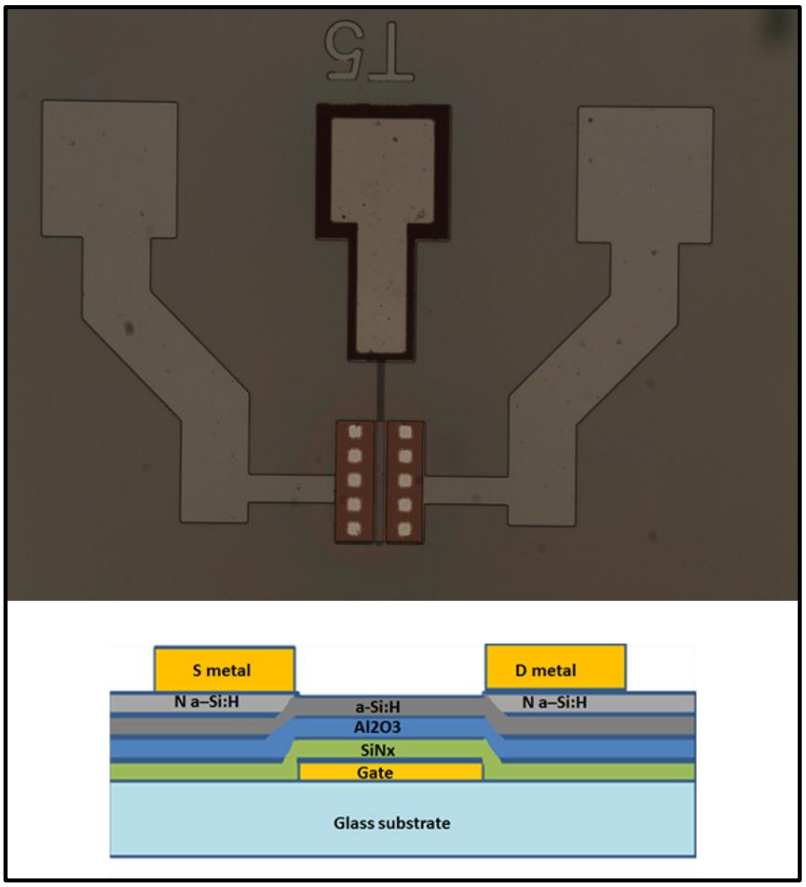

Figure 4.14: Photomicrograph and schematic cross-sectional view of the final TFT device after M2 step (the gate length is 10 microns in photomicrograph).

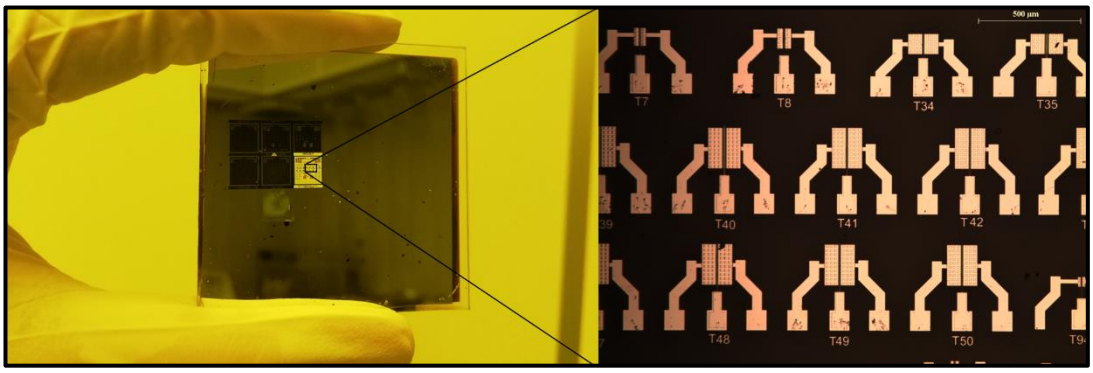

Figure 4.15: (a) the fabricated sample, (b) the TFT array on the glass substrate.

4.2. Electrical Characterization of the Devices

The electrical characterization of the microdevices on the fabricated samples was conducted. The electrical measurements obtained from the top-gate and the bottom-gate transistors and the results of the electrical calculations for the top-gate devices are given below.

4.2.1. TFT Electrical Measurements

Electrical measurement results for top-gate and bottom-gate devices are as follows.

Top-gate TFT I-V results (effect of vacuum annealing on device characteristics);

For device with W/L = 100/5 (T34_2);

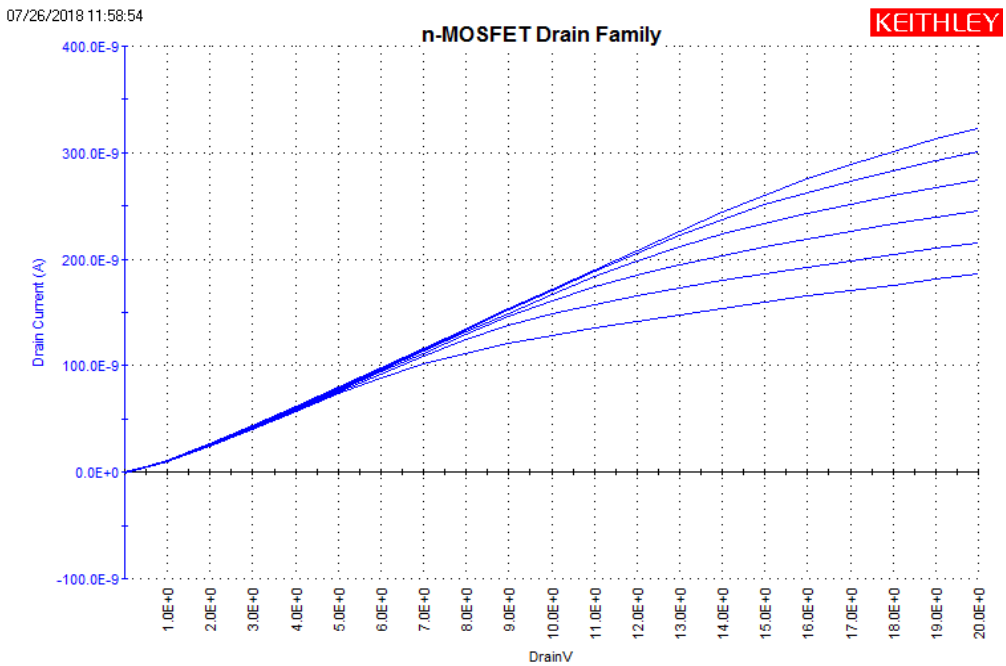

Figure 4.16: I_d-V_{ds} characteristics (V_{gs} = 0, 1, 2, 3, 4, 5V) 150°C vacuum annealing.

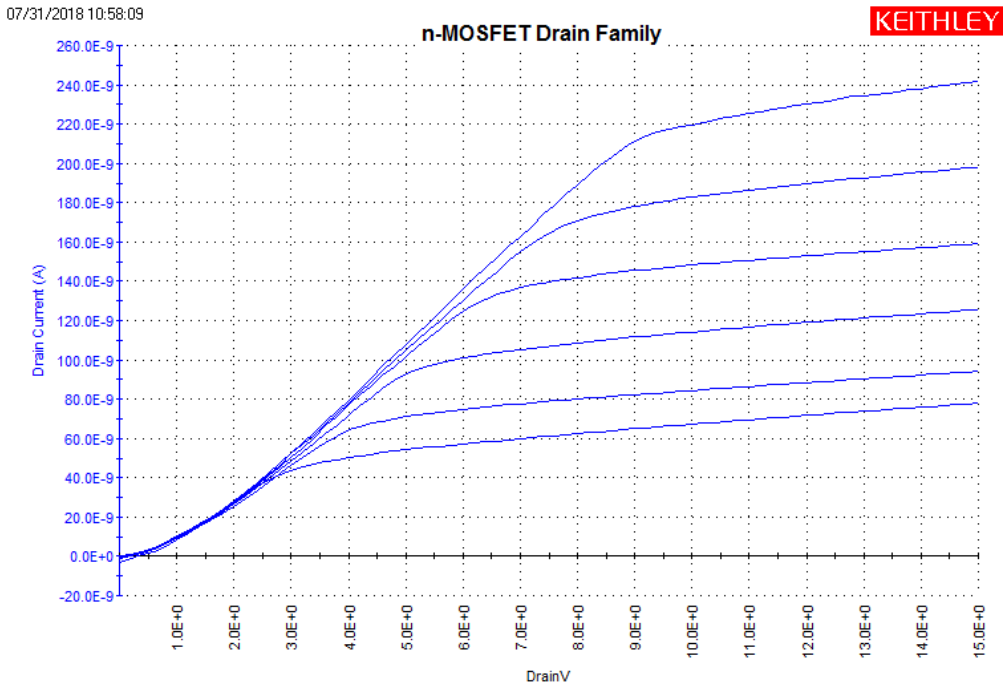

Figure 4.17: I_d-V_{ds} characteristics (V_{gs} = 1, 2, 3, 4, 5, 6V) 200°C vacuum annealing.

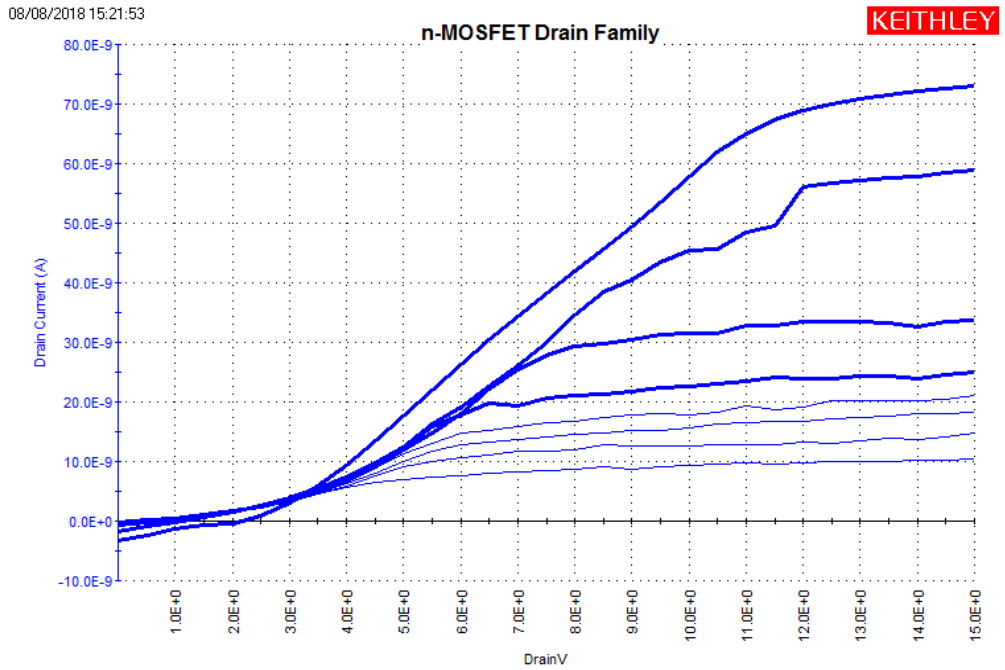

Figure 4.18: I_d-V_{ds} characteristics (V_{gs} = 1, 2, 3, 4, 5, 6V) 250°C vacuum annealing.

For device with W/L = 100/5 (T8);

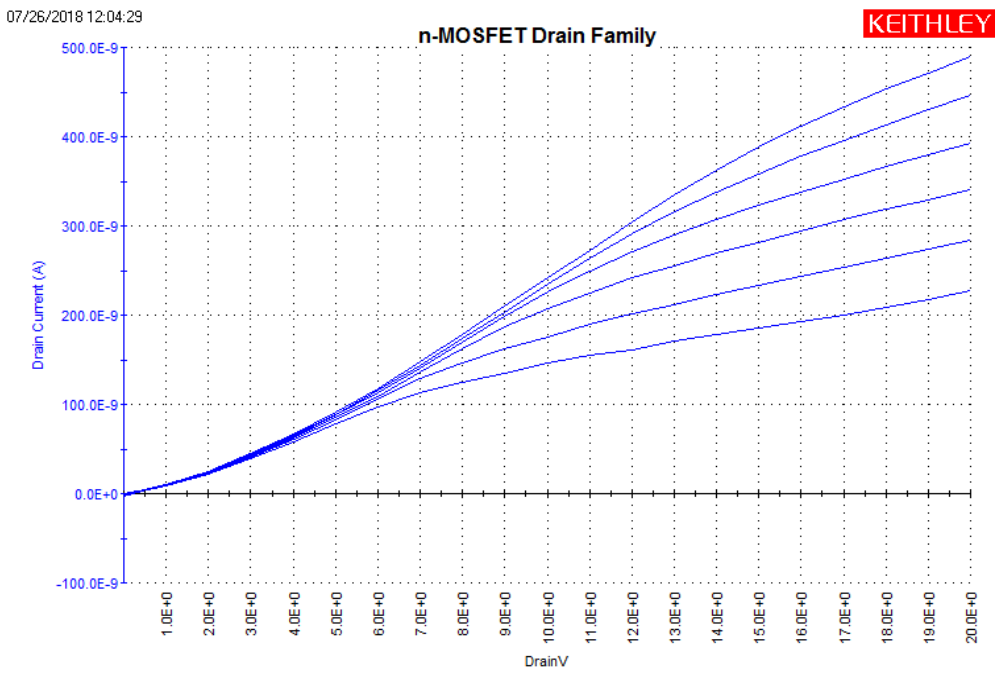

Figure 4.19: I_d-V_{ds} characteristics (V_{gs} = 0, 1, 2, 3, 4, 5V) 150°C vacuum annealing.

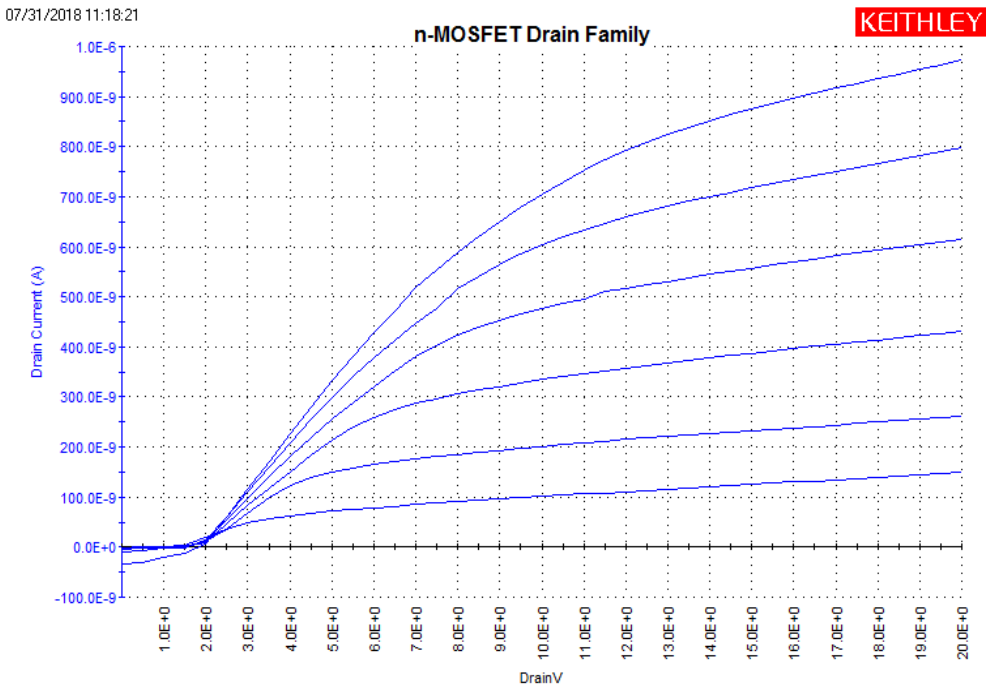

Figure 4.20: I_d-V_{ds} characteristics (V_{gs} = 1, 2.8, 4.6, 6.4, 8.2, 10V) 200°C vacuum annealing.

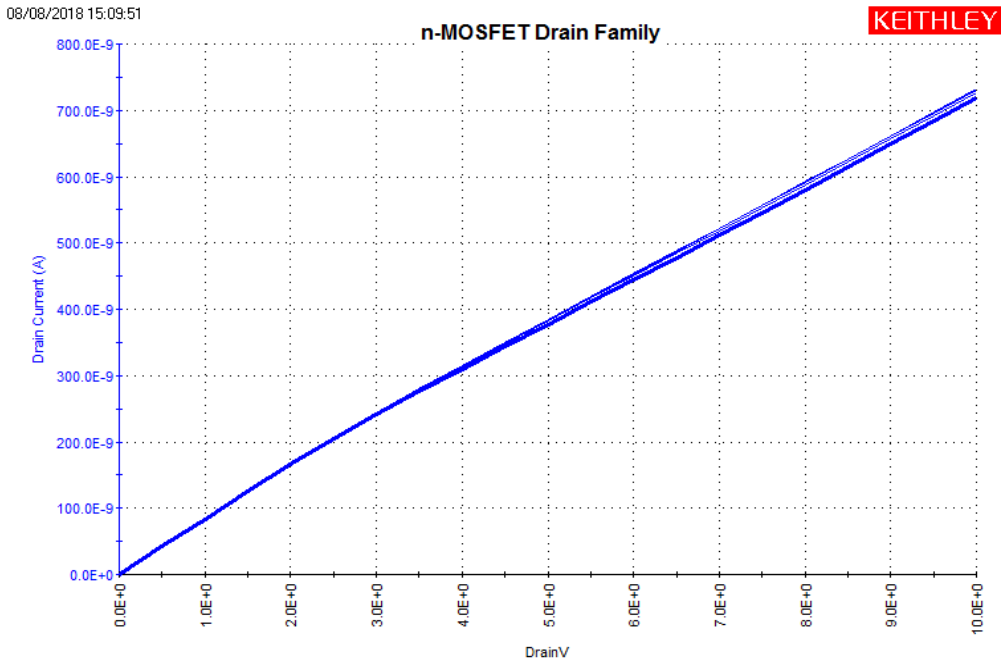

Figure 4.21: I_d-V_{ds} characteristics (V_{gs} = 1, 2, 3, 4, 5V) 250°C vacuum annealing.

For device with W/L = 800/6 (T31_2);

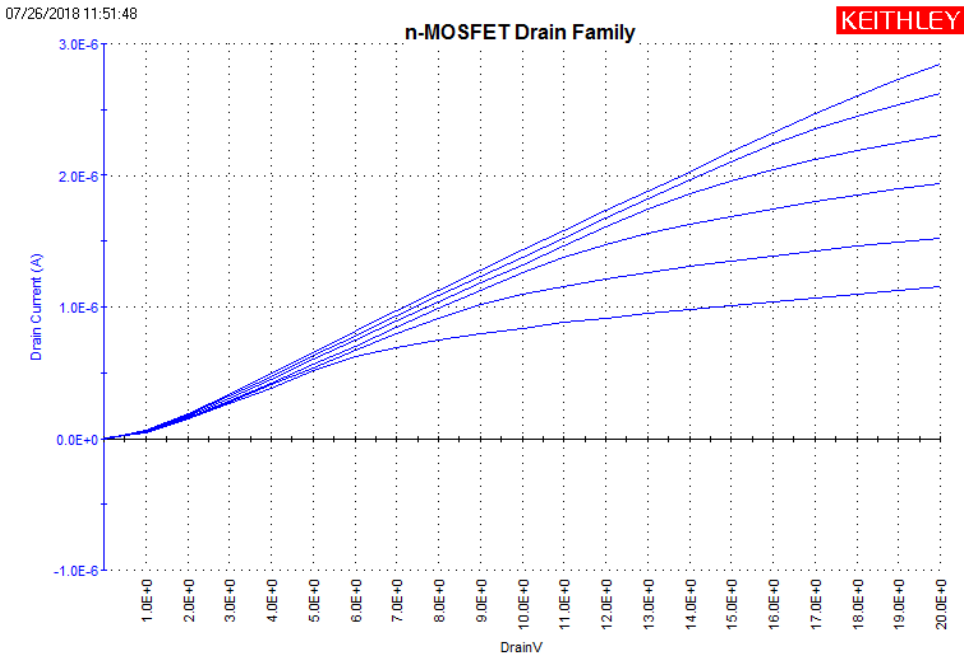

Figure 4.22: I_d-V_{ds} characteristics (V_{gs} = 1, 2.8, 4.6, 6.4, 8.2, 10V) 150°C vacuum annealing.

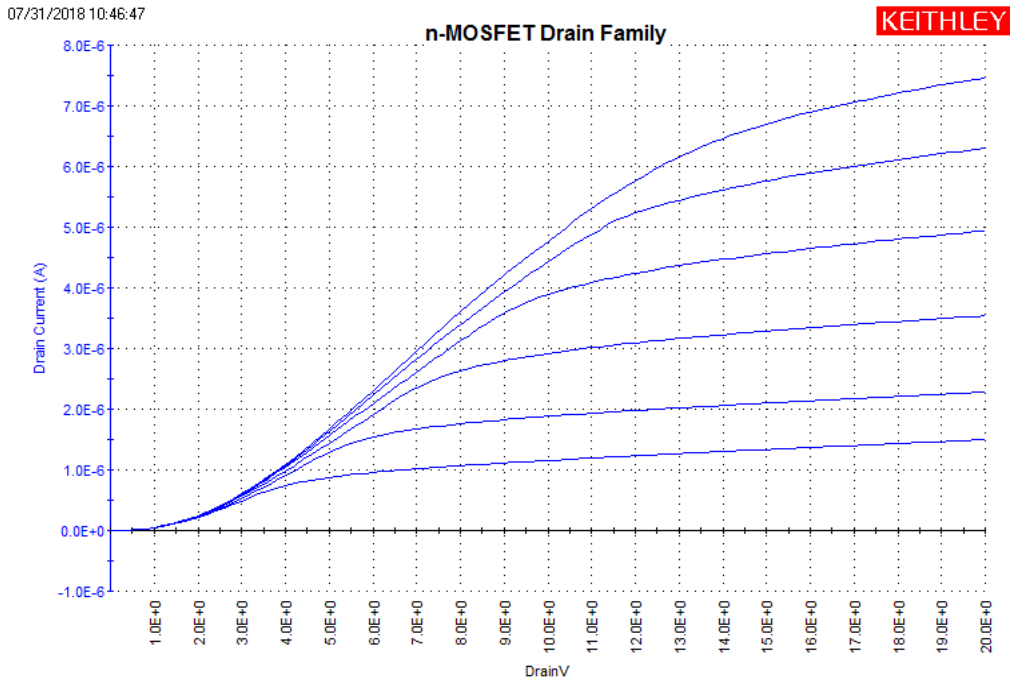

Figure 4.23: I_d-V_{ds} characteristics (V_{gs} = 1, 2.8, 4.6, 6.4, 8.2, 10V) 200°C vacuum annealing.

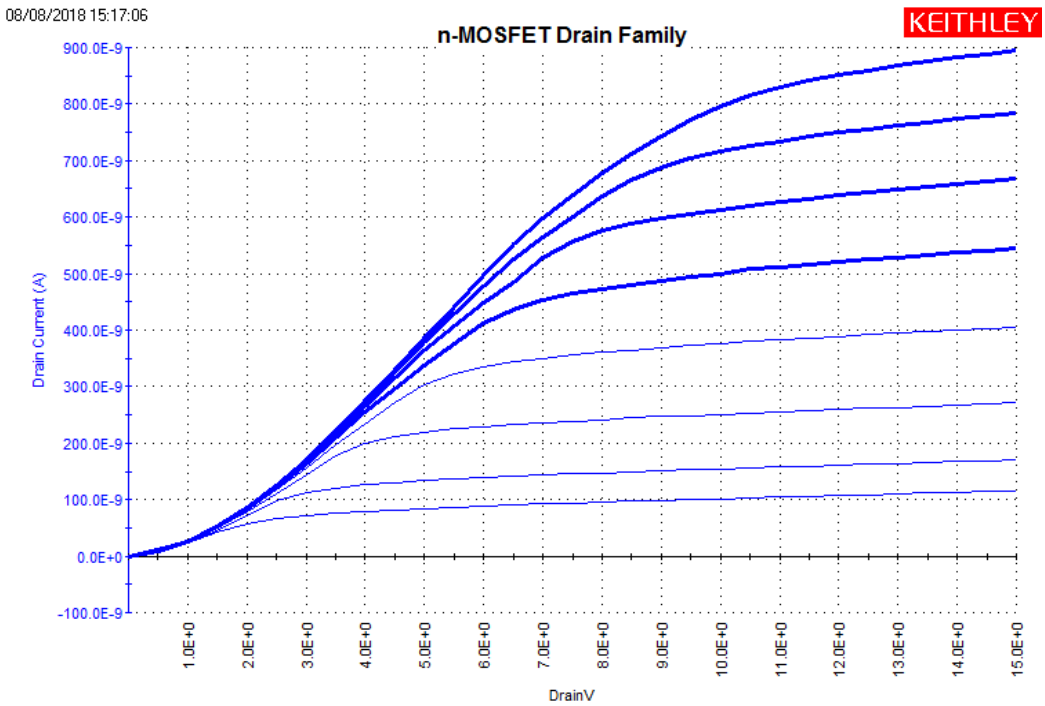

Figure 4.24: I_d-V_{ds} characteristics (V_{gs} = 1, 2.8, 4.6, 6.4, 8.2, 10V) 250°C vacuum annealing.

Bottom-gate TFT I-V results;

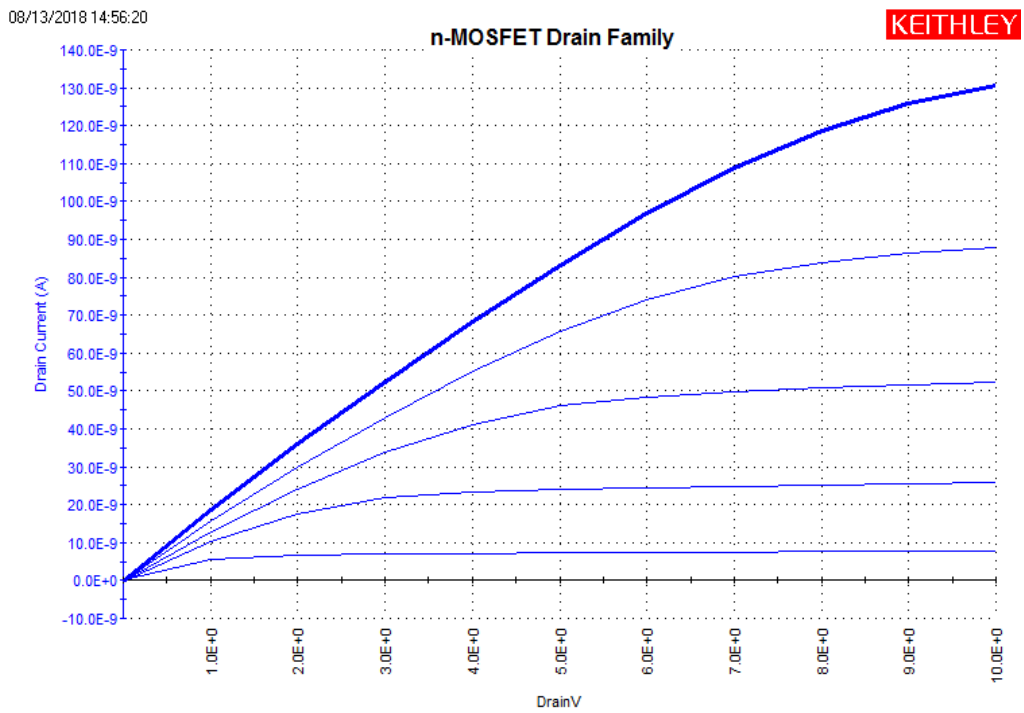

Figure 4.25: I_d-V_{ds} characteristics (V_{gs} = 1, 2.8, 4.6, 6.4, 8.2, 10V).

The transistor characteristics improved after post heating of the samples. This improvement may be due to the removal of defects between the interlayers and the diffusion of the metal layer into the active layer. But we can lose our transistor at further heating as seen at Figure 4.21.

Bottom gate TFTs generally exhibit lower drain current levels but are better at the saturation region, however, for the application where the devices will be used, the linear region is more important because it will generally be used at low voltages as switching transistors but for driving TFT we need its saturation region.

4.2.2. TFT Electrical Calculations

In this section, mobility calculations based on TFT electrical measurements for top-gate devices are given.

In semiconductors, mobility is as important as the charge carrier. It determines whether the semiconductor is used as a circuit element.

q: Charge carrier [C]

μ: Mobility [cm^2/Vs]

n: Carrier concentration [m^{-3}] (The number of charge carriers in per volume)

$$\sigma \text{ (Conductivity)} = qn\mu \tag{4.1}$$

1) Mobility formulas: Mobility is calculated from the linear region and the saturation region (Figure 4.26). The mobility formulas for both regions are as follows.

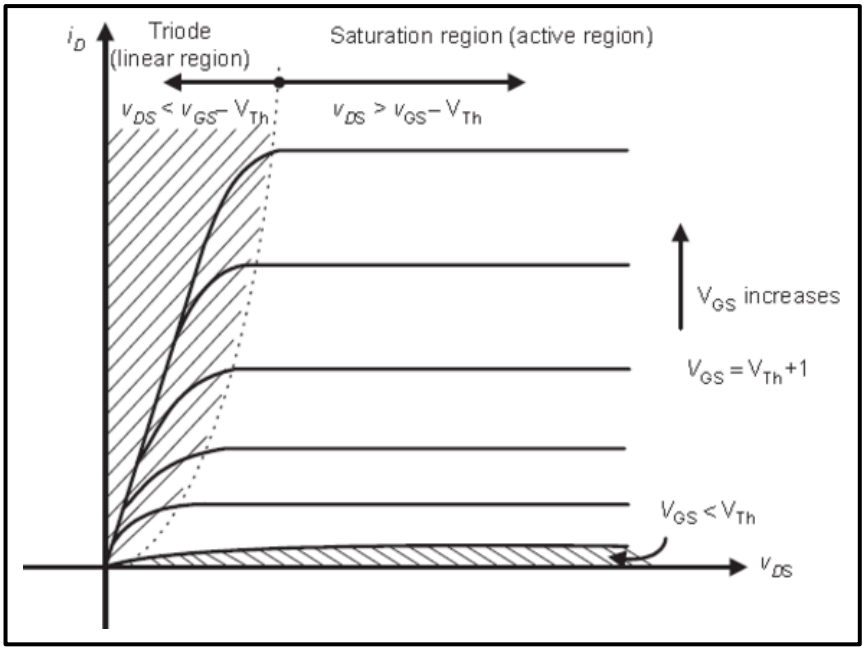

Figure 4.26: I_d-V_{ds} graph (linear vs. saturation region).

The I-V equations for the linear region and the saturation region are as follows. For the linear region;

$$I_d = \frac{W}{L}\,\mu\, C_{ox}\left[\left(V_{gs} - V_t\right) - \frac{V_{ds}}{2}\right] V_{ds} \tag{4.2}$$

$$I_d = \frac{W}{L}\,\mu\, C_{ox}\left[\left(V_{gs} - V_t\right) V_d - \frac{V_{ds}^2}{2}\right] \tag{4.3}$$

For $V_{ds} \ll (V_{gs} - V_t)$;

$$I_d = \frac{W}{L} \mu C_{ox} \left[(V_{gs} - V_t)\right] V_{ds} \tag{4.4}$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}}, \mu = \frac{L\, g_m}{W\, C_{ox}\, V_{ds}} \tag{4.5, 4.6}$$

$$C_{ox} = \frac{E_0\, E}{t} \tag{4.7}$$

For the saturation region;

For $V_{ds} \gg (V_{gs} - V_t)$;

$$I_d = \frac{W}{2L} \mu C_{ox} (V_{gs} - V_t)^2 \tag{4.8}$$

$$g_m = \frac{\sqrt{\partial I_d}}{\partial V_{gs}} \tag{4.9}$$

$$C_{ox} = \frac{E_0\, E}{t} \tag{4.10}$$

μ: Electron mobility

I_d: Drain current

W: Channel width

L: Channel length

V_{gs}: Gate-Source voltage

V_t: Threshold voltage

V_{ds}: Drain-Source voltage

C_{ox}: Gate capacitance

E_0: Dielectric constant of vacuum medium

E: Dielectric coefficient of thin film material

t: Thin film thickness

Another method for calculating mobility of the saturation region is as follows.

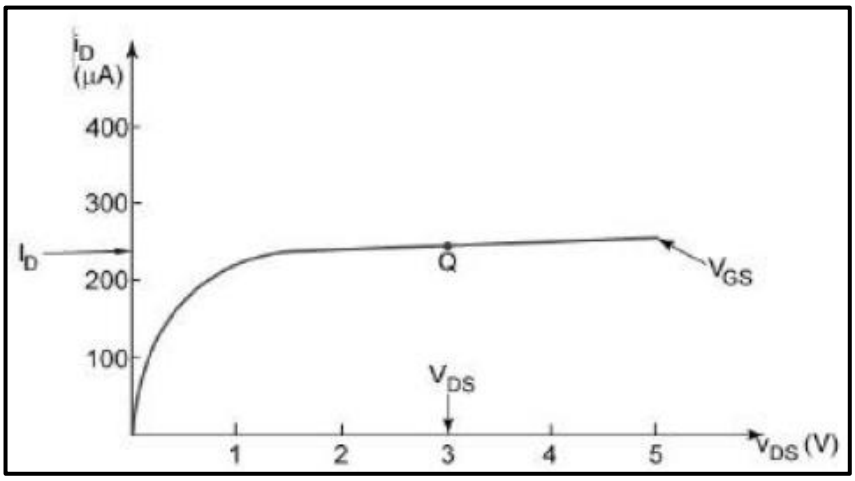

Figure 4.27: I_d-V_{ds} graph (Q point).

As in the I_d-V_{ds} graph given in Figure 4.27, mobility is calculated from the Q working region, that is, I_d, V_{ds}, and V_{gs} values at the point where the current is constant. The mobilities of T8, T31_2, and T34_2 transistors were calculated by this method.

2) Channel length modulation: When V_{ds} reaches the value of V_{gs}–V_t, the channel becomes pinch-off and the I_d current reaches saturation. From this point on; when V_{ds} is increased, I_d will remain constant. However, in practice, increase of V_{ds} larger than V_{gs}–V_t leads shorter channel effective length. This results in a further increase in the I_d current. This effect is called channel length modulation (Figure 4.28).

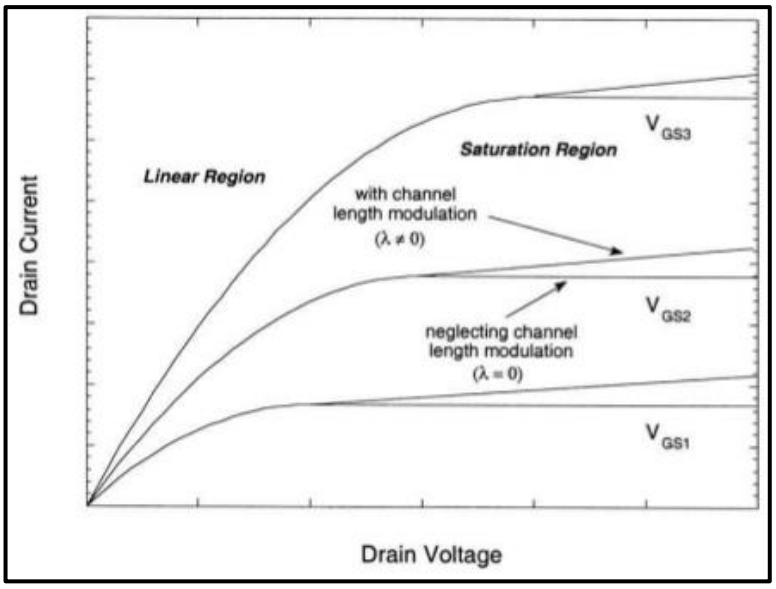

Figure 4.28: I_d-V_{ds} graph (effect of channel length modulation).

Electrical properties in channel length modulation are as follows.

For the linear region;

For $V_{ds} \ll (V_{gs} - V_t)$;

$$I_d = \frac{W}{L}\,\mu\, C_{ox}\left[(V_{gs} - V_t)\right] V_{ds}\,[1 + \lambda V_{ds}] \tag{4.11}$$

For the saturation region;

For $V_{ds} \gg (V_{gs} - V_t)$;

$$I_d = \frac{W}{2L}\,\mu\, C_{ox}\,(V_{gs} - V_t)^2\,[1 + \lambda V_{ds}] \tag{4.12}$$

The λ (lambda) term in these relations is called the channel length modulation parameter. Lambda magnitude is a magnitude defined in a similar manner to Early voltage which models Early phenomenon in BJT (Figure 4.29). The channel length modulation parameter is expressed as $\lambda = 1/V_A$.

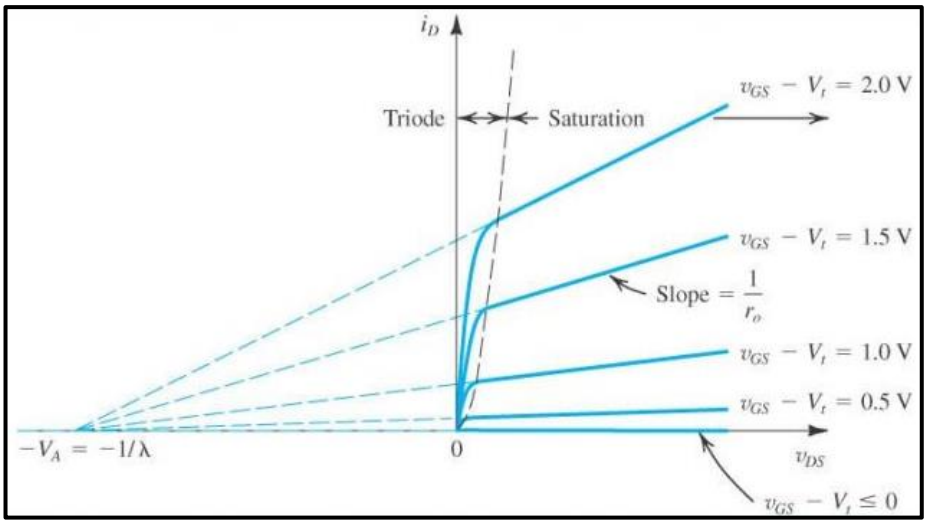

Figure 4.29: I_d-V_{ds} graph (Early effect).

3) Calculation of gate capacitance in different dielectric materials: In order to improve characterizations such as mobility and speed in semiconductor materials, dielectric materials with different structures are used. In different dielectric materials of different thickness, C_{ox} (gate capacitance) is calculated as follows;

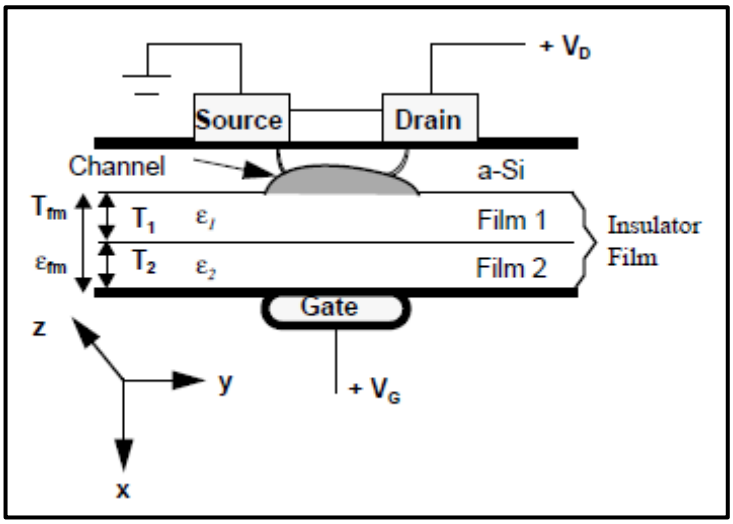

Figure 4.30: TFT device with bilayer gate dielectric structure.

$$C_{ox} = \frac{E_0\, E_1\, E_2}{t_1\, E_2 + t_2\, E_1} \tag{4.13}$$

E_0: Dielectric constant of vacuum medium

E_1: Dielectric coefficient of film 1 material

E_2: Dielectric coefficient of film 2 material

t_1: Film 1 thickness

t_2: Film 2 thickness

C_{ox}: Gate capacitance

200 nm SiN_x and 50 nm Al_2O_3 were used as the gate dielectric materials of transistors T8, T31_2, and T34_2.

Table 4.2: Gate capacitance calculation.

t_1 (SiN_x) [m]	t_2 (Al_2O_3) [m]	E_1 (SiN_x) [F/m]	E_2 (Al_2O_3) [F/m]	E_0 [F/m]	C_{ox} [F/m^2]
2,00E-07	5,00E-08	7,5	9,5	8,85E-12	2,7730E-04

The gate capacitance value of transistors T8, T31_2, and T34_2 is C_{ox}=2,7730E-04 F/m^2 (Table 4.2).

4) Mobility calculations of T8, T31_2, and T34_2 transistors: Since $\partial I_d/\partial V_{gs}$ slopes were not linear for small V_{ds} values in the linear region, mobility was calculated for the saturation region.

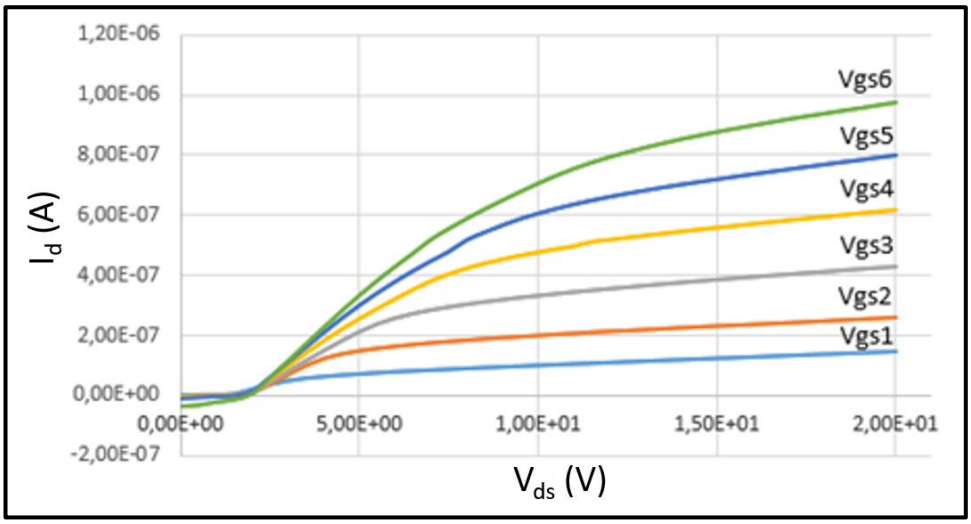

Figure 4.31: I_d-V_{ds} graph (T8).

Table 4.3: V_{gs} values (T8).

V_{gs1} (V)	V_{gs2} (V)	V_{gs3} (V)	V_{gs4} (V)	V_{gs5} (V)	V_{gs6} (V)
1	2,8	4,6	6,4	8,2	10

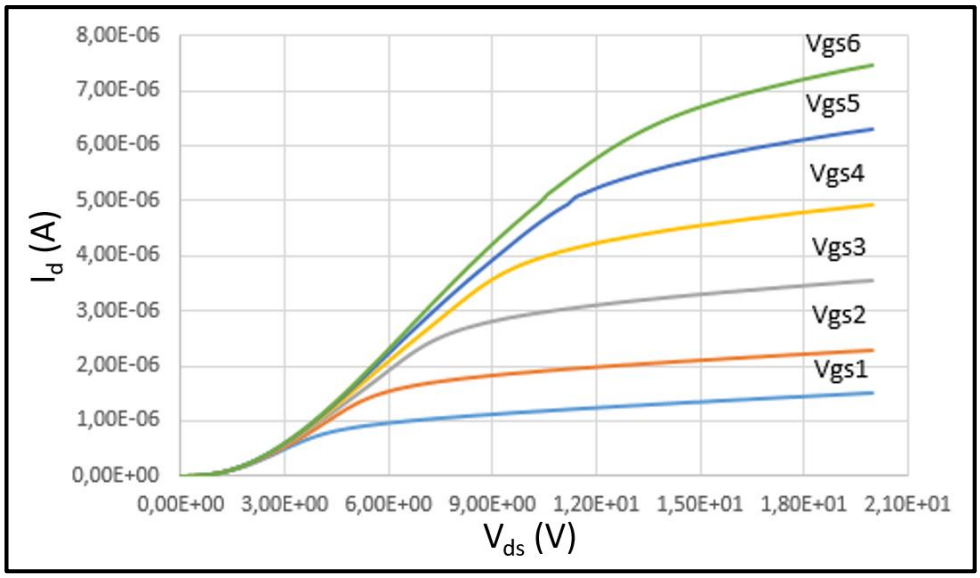

Figure 4.32: I_d-V_{ds} graph (T31_2).

Table 4.4: V_{gs} values (T31_2).

V_{gs1} (V)	V_{gs2} (V)	V_{gs3} (V)	V_{gs4} (V)	V_{gs5} (V)	V_{gs6} (V)
1	2,8	4,6	6,4	8,2	10

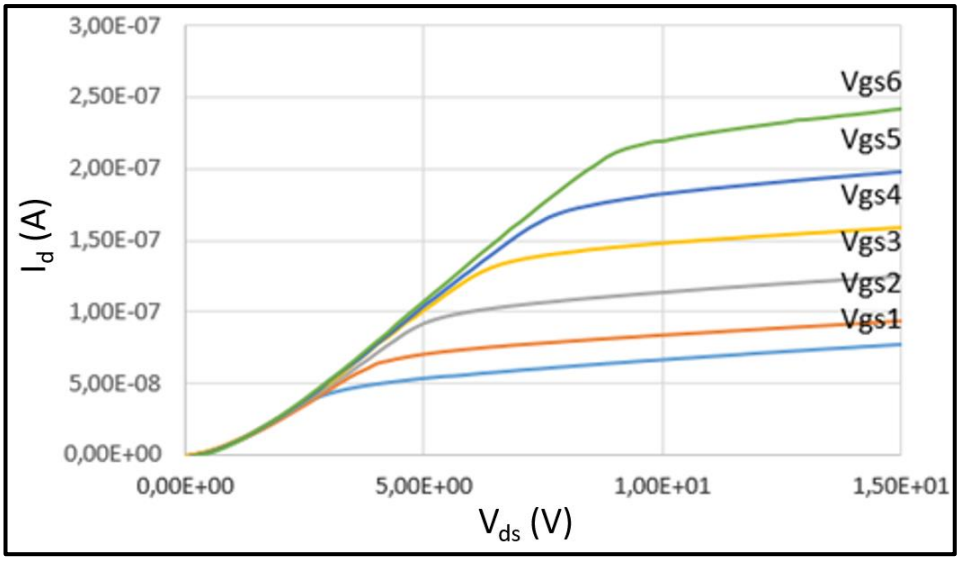

Figure 4.33: I_d-V_{ds} graph (T34_2).

Table 4.5: V_{gs} values (T34_2).

V_{gs1} (V)	V_{gs2} (V)	V_{gs3} (V)	V_{gs4} (V)	V_{gs5} (V)	V_{gs6} (V)
1	2	3	4	5	6

Table 4.6: Mobility calculation.

	W [µm]	**L [µm]**	**C_{ox} [F/m^2]**	**V_t [V]**	**λ [V]**	**µ [cm^2 V^{-1} s^{-1}]**
T8	100	5	2,7730E-04	0,9	0,05	0,059
T31_2	800	6	2,7730E-04	0,9	0,05	0,077
T34_2	100	5	2,7730E-04	0,9	0,05	0,037

The mobility values obtained by using the saturation region in the TFTs fabricated ranged from 0.04–0.08 cm^{2}V^{-1}s^{-1} (Table 4.6). This calculated mobility is the field effect mobility and varies according to the device parameters. Mobility values can be increased as the post annealing optimization is improved. We can also use lightly doped N region as the channel layer, but this process is very difficult to control. We can also use different metals for the source and drain to decrease the threshold voltage.

5. CONCLUSION

The large area electronics especially display technology got momentum with the introduction of thin-film transistor devices. Due to its capability of uniform deposition over a large substrate, low deposition temperatures, standard fabrication processes, and low costs, a-Si:H technology is attractive in large area applications. The most appealing applications of amorphous silicon TFTs are liquid crystal displays and, most recently, organic light emitting diode displays. The purpose of this study is to develop amorphous silicon based thin-film transistors for large area electronics, especially AMOLED applications. In accordance with this purpose, we have successfully fabricated a-Si:H TFTs with top-gate and bottom-gate configurations. The I_d-V_{ds} characteristics for the fabricated devices were obtained and studied.

We got drain current on the order of 5 micro ampere, the turn on/off ratio of 10^6 for the current. Field effect mobility of approximately 0.08 $cm^2V^{-1}s^{-1}$ was obtained from some of the devices. Threshold voltages of 5–10 volts were measured from the I_d-V_{gs} curves. From these results, these TFTs proved to be used in AMOLED applications.

We would like to improve the fabrication steps so that less masks are needed, and the cleaning procedures will be applied. Different metals will be used as the contact metals to decrease the threshold voltage having lower work function.

We plan to use laser crystallization method to increase the mobility of the channel layer so that we can also increase the field effect mobility as well.

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